CD1005 INDUSTRIAL DIGITAL ELECTRONIC DETONATOR CONTROL CHIP

Shanghai ChipDance Co., Ltd.

Contents

1 Basic Information

1.1 Functional Introduction

CD1005 chip is an industrial digital electronic detonator control chip launched by Shanghai Chipdance Technology Co., Ltd. It can control the energy storage capacitor, ignition switch and other peripheral devices on the electronic detonator module according to the instructions sent by the detonator through the bus, and realize large-scale, high-precision timing detonation.

CD1005 has the following features:

- It can support busbars with a length of more than 2,000 meters and realize the networking of more than 1,000 detonators;
- It can store key information such as UID, shell code, detonation password, etc. of electronic detonators and lock them;
- It provides the function of verifying the detonation password, and detonation can only be performed when the verification is passed;
- It provides 9 voltage values, which can accurately control the voltage of the energy storage capacitor;
- The extension time can be stored in advance or programmed on site, with a maximum of about 65 seconds and a minimum interval of 1ms;
- It optimizes the programming, verification, and confirmation processes for on-site detonation, and shortens the time required for on-site detonation while minimizing the risk of misfires and rejections;
- It supports the operation process of networking first and then registering, simplifying the use process in specific scenarios;
- It optimizes the interference from the bus to improve the reliability in specific scenarios;
- The chip integrates the function of checking the connectivity of the energy storage capacitor and the lead resistor;
- The module only requires 8 peripheral devices (including the energy storage capacitor and the lead resistor), and the integration is extremely high.

1.2 Key Features

Table 1.1 Key functional indicators of CD1005

Symbol	Parameter definition	Unit	Minimum	Typical	Maximum
V_{A-B}	AB bus supply voltage	V	6.5	10.0	40.0
T_j	Chip operating temperature	℃	-40	25	85
I_{A-B} (idle)	Bus current in standby state (VA-B=10V)	μA	13.0	16.5	20.0
V_{VCHG} (target)	Target voltage corresponding to charging gear (3~5V gear)	V	Gear voltage ±0.2		
V_{VCHG} (target)	Target voltage corresponding to charging gear (10~22V gear)	V	Gear voltage ±2.5%		
ΔV_{VCHG}	Fluctuation range of VVCHG after full charge (CVCHG≥33μF)	mV	--	--	50
I_{VCHG} (delay)	VCHG current during delay (VVCHG=20V, VA-B=0V)	μA	10.0	12.0	14.0
T_{DELAY}	Programmable delay value range*	ms	0	--	65,534
T_err_{delay}	Delay time error (Tdelay≤150ms)	μs	-300	--	300
T_err_{delay}	Delay time error (Tdelay>150ms)	‰	-2	--	2

*The programmable delay value range does not represent the actual available delay value range. The actual maximum available delay value can be obtained by simple calculation based on the current consumed by the chip during delay, the capacitance and leakage current of the energy storage capacitor, the charging voltage, and the minimum voltage required for the detonating charge head. For example, if the minimum capacity of the energy storage capacitor is 33uF, the maximum leakage current of the energy storage capacitor is 5μA, the charging voltage of the energy storage capacitor is 18V, and the minimum voltage required for the detonating charge head is 11V, then the actual maximum available delay value tmax in this case is:

$$t_{max} = \frac{33\mu F \times (18V - 11V)}{14\mu A + 5\mu A} \approx 12.2s$$

1.3 Pin definition

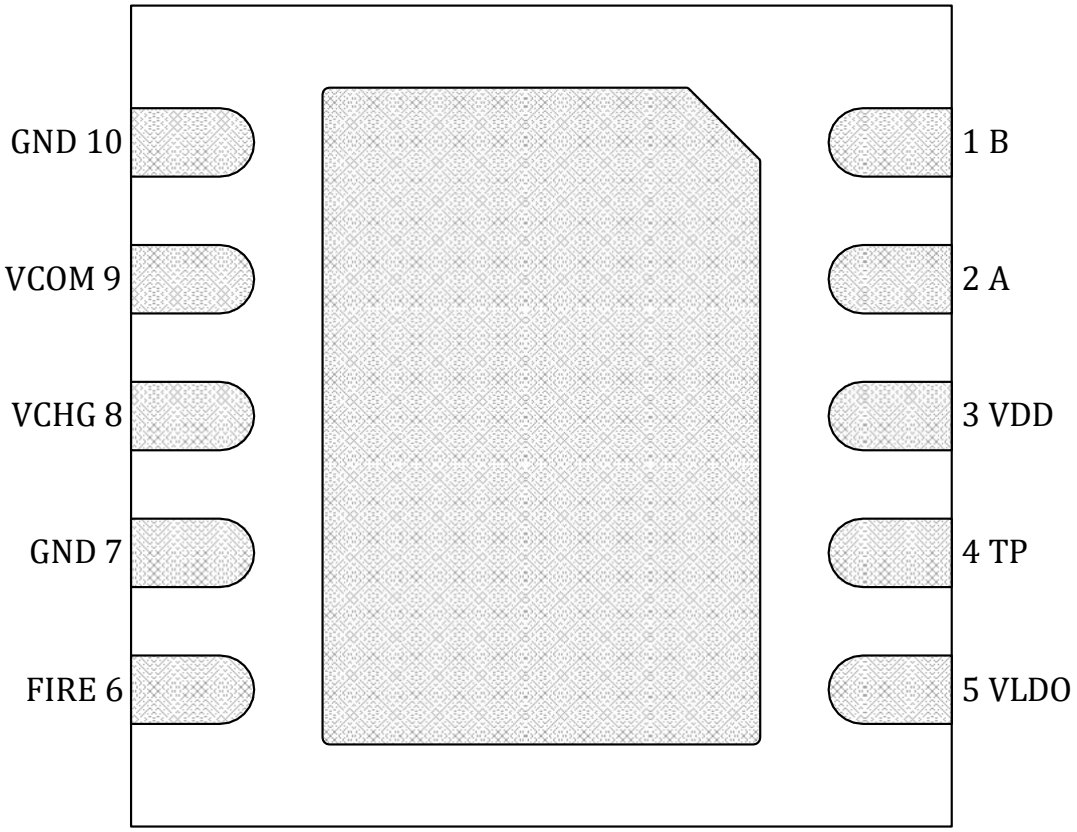

Figure 1.1 Package bottom view

Table 1.2 Pin definition

Number	Name	Type	Definition
1	B	Analog input, power supply	B bus signal input, power supply
2	A	Analog input, power supply	A bus signal input, power supply
3	VDD	Power supply	On-chip rectifier bridge output
4	TP	Analog output	Test pin
5	VLDO	Power supply	On-chip low voltage power supply, external filter capacitor
6	FIRE	Digital output	NMOS ignition switch control signal
7	GND	Ground	Ground
8	VCHG	Power supply, analog output	Energy storage capacitor charging pin, resistance current output
9	VCOM	Power supply	On-chip high voltage power supply, external communication capacitor
10	GND	Ground	Ground

1.4 Package Appearance

The specific appearance dimensions of the DFN3×3-10L package used by the CD1005 chip are given inTable 1.3 ANDFigure 1.2 .

Table 1.3 CD1005 DFN3×3-10L package dimensions (unit: mm)

Legend	Minimum value	Typical value	Maximum value	Legend	Minimum value	Typical value	Maximum value	Legend	Minimum value	Typical value	Maximum value
A	0.700	0.750	0.800	E	2.900	3.000	3.100	b	0.180	0.230	0.300
A1	0.000	0.020	0.050	D1	2.400	2.500	2.600	e	0.500 BSC		
A3	0.203 REF			E1	1.450	1.550	1.650	Ne	2.000 BSC		
D	2.900	3.000	3.100	h	0.200	0.250	0.300	L	0.300	0.400	0.500

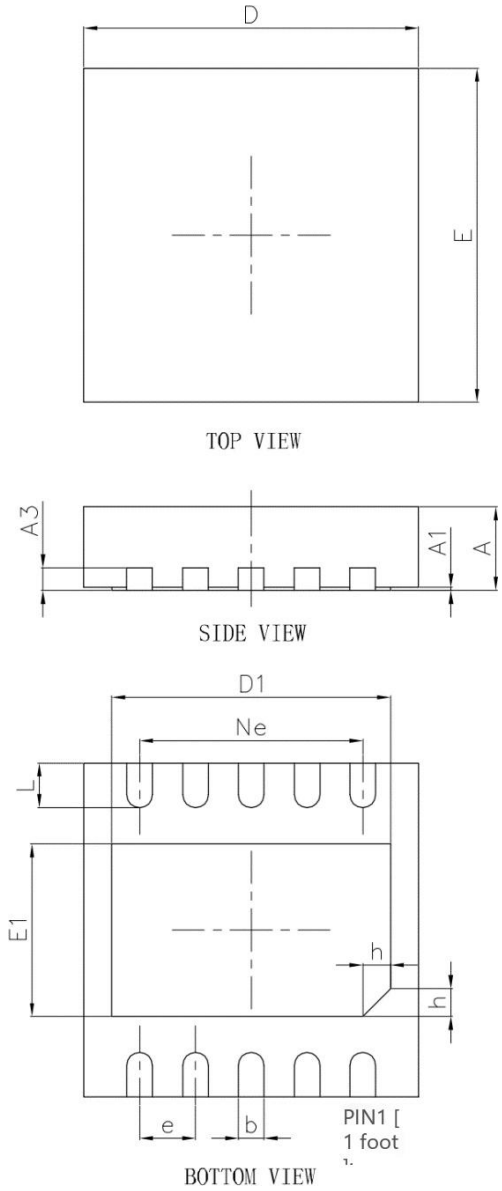

Figure 1.2 CD1005 DFN3×3-10L package dimensions

1.5 Typical Design Scheme of Electronic Detonator Module

Figure 1.3 is the most simplified reference design scheme of the electronic detonator module with a single ignition switch package using the CD1005 chip, where LINE_A and LINE_B are the inputs of bus A and B, YT is the lead resistor, C1 is the energy storage capacitor, C2 is the communication capacitor, C3 is the low-voltage power supply filter capacitor, Q1 is the NMOS ignition switch, and D1 is the TVS diode for surge protection. It can be seen that the module only requires 8 peripheral devices, including the lead resistor and the energy storage capacitor, and the integration is extremely high.

When designing the module PCB, it should be noted that in order to facilitate testing, test contacts should be designed at both ends of the lead resistor.

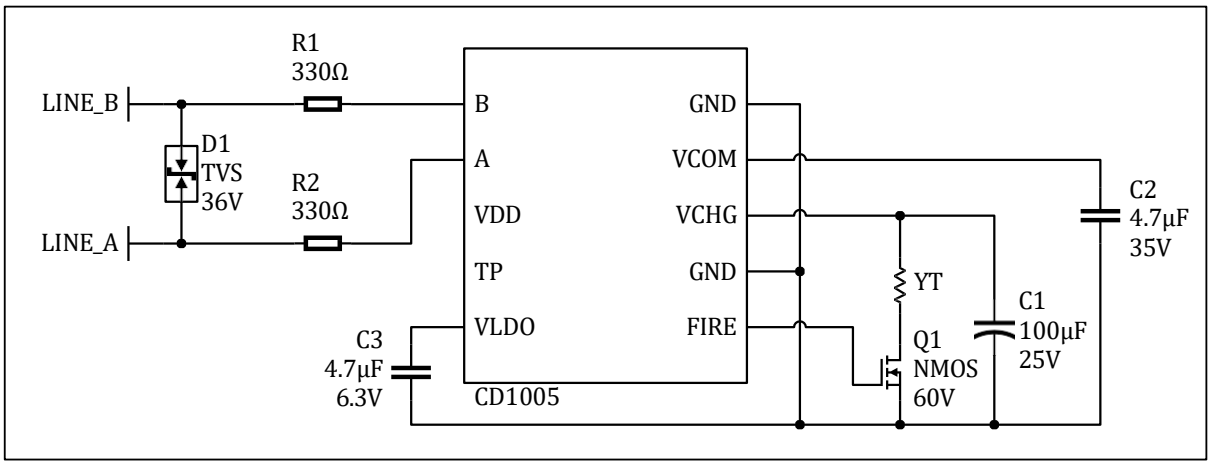

Figure 1.3 The most simplified module scheme

12 Electrical Characteristics

12.1 DC electrical characteristics

Table 2.1 CD1005 DC electrical characteristics parameters

Symbol	Parameter definition	Unit	Minimum value	Typical value	Maximum value
Power supply electrical characteristics					
V_{A-B}	AB bus power supply voltage	V	6.5	10.0	40.0
V_{drop}	Voltage drop from AB bus power supply voltage to on-chip high voltage power supply	V	2.1	2.5	3.0
V_{VCOM}	On-chip high voltage power supply (communication capacitor) voltage	V	V_{A-B} - V_{drop}		
V_{VLDO}	On-chip low voltage power supply voltage (VA-B=10V)	V	2.9	3.0	3.1
I_{A-B} (idle)	Bus current in standby state (VA-B=10V)	μA	13.0	16.5	20.0
Communication function related electrical characteristics					
T_{osc}	On-chip clock oscillator period	μs	4.54	5.00	5.56
R_{A-B} (fb.)	Equivalent resistance in chip during feedback (VA-B=10V)	Ω	210	300	390
Charge/discharge function related electrical characteristics					
V_{VCHG} (target)	Target voltage corresponding to charging gear (3~5V gear)	V	Gear voltage ±0.2		
V_{VCHG} (target)	Target voltage corresponding to the charging gear (10~22V gear)	V	Gear voltage ±2.5%		
ΔV_{VCHG}	Fluctuation range of VVCHG after full charge (CVCHG≥33μF)	mV	--	--	50
$I_{int.}$ (chg.)	Current consumed by the chip itself during charging (VA-B=28V)	μA	20.0	25.0	30.0
$I_{int.}$ (chgd.)	Current consumed by the chip itself after full charge (VVCHG=20V)	μA	16.0	21.0	26.0
I_{VCHG} (chg.)	Current of VCHG during charging (VA-B=28V)	mA	--	--	1.5
I_{VCHG} (dchg.)	Current of VCHG during discharge (VVCHG=20V)	mA	--	--	15
Electrical characteristics related to the delay function					
I_{VCHG} (delay)	VCHG current during delay (VVCHG=20V, VA-B=0V)	μA	10.0	12.0	14.0
T_err_{delay}	Error of delay time (Tdelay≤150ms)	μs	-300	--	300
T_err_{delay}	Error of delay time (Tdelay>150ms)	‰	-2	--	2
Electrical characteristics related to the measurement function					
I_{VCHG} (mea.)	Current output when measuring resistance	mA	0.8	0.9	1
$V_{res.\ open}$	Reference voltage for judging open circuit resistance (configuration area 0.3V)	mV	150	250	350
R_{open}	Open circuit resistance threshold	Ω	150	278	438
C_{open} (max.)	Maximum value of open circuit capacitance threshold (parameter T=7, 3V position)	μF	8	13	17
C_{open} (min.)	Minimum value of open circuit capacitance threshold (parameter T=0, 5V position)	nF	270	430	560

2.2 Maximum Withstand Voltage

Table 2.2 Maximum withstand voltage of each pin of CD1005

Symbol	Parameter definition	Unit	Minimum value	Typical value	Maximum value
VCHG	Energy storage capacitor charging pin, resistance current output	V	--	--	32
VCOM	On-chip high voltage power supply, external communication capacitor	V	--	--	45
B	B bus signal input	V	--	--	45
A	A bus signal input	V	--	--	45
VLDO	On-chip low voltage power supply, external filter capacitor	V	--	--	7
TP	Test pin	V	--	--	7
FIRE	NMOS ignition switch control signal	V	--	--	7

3 Internal Structure of the Chip

3.1 Overall Architecture of the Chip

The main functional modules in the CD1005 chip and the relationship between these modules are shown inFigure 3.1 .

The red box in the figure represents the high-voltage module (powered by the bus, VCOM or VCHG), and the blue box represents the low-voltage module (powered by the on-chip LDO low-voltage power supply).

The red line in the figure represents the power supply, the blue line represents the analog signal, the green line represents the digital signal, and the arrow direction on the line represents the signal direction.

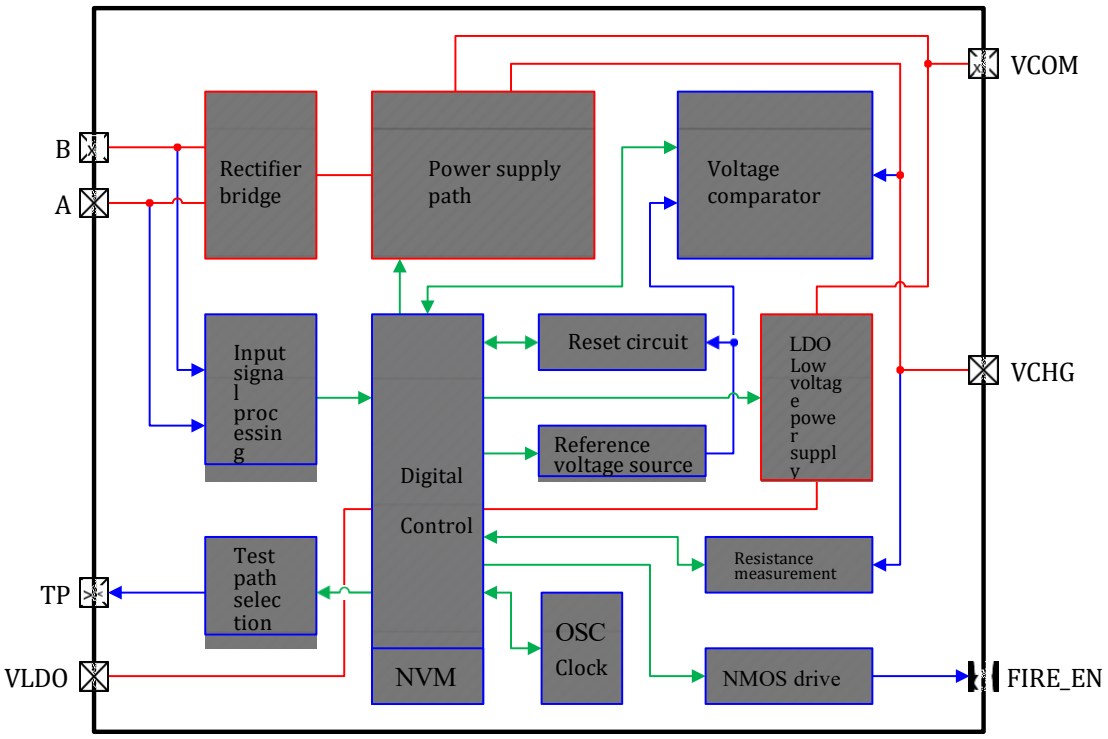

Figure 3.1 Schematic diagram of the main modules and their mutual relationship

3.2 Power Supply Path

The power supply path module includes feedback switch, bus power switch, charge/discharge switch, communication capacitor power supply path and other parts, which are briefly described in this section.

3.2.1 Feedback switch and bus power switch circuit

The circuit schematic diagram of the feedback switch and bus power switch part in the CD1005 chip is shown inFigure 3.2Among them, CF-IN is the internal signal of the control feedback tube, and HDSW-ENB is the internal signal of the control bus power switch tube. Q1 is a feedback switch transistor, an NMOS transistor with a nominal withstand voltage of 60V; Q2 is the bus power switch tube, which is nominal

NMOS transistor with a withstand voltage of 60V; Q3 is the control transistor for the bus power switch, which is an NMOS transistor with a nominal withstand voltage of 40V; Q4 is a pull-down transistor that works in conjunction with the bus power switch and is an NMOS transistor with a nominal withstand voltage of 50V.

The nominal resistance of R1 is 60Ω, the nominal resistance of R2 is 208Ω, and the nominal resistance of R3 is 8MΩ.

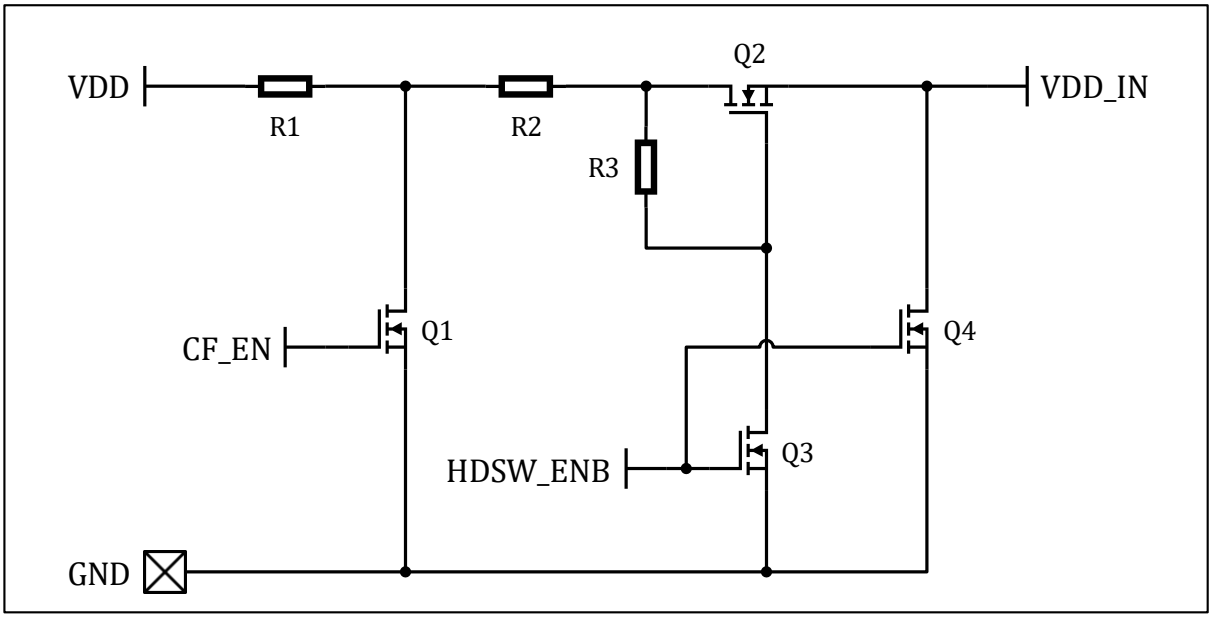

Figure 3.2 Schematic diagram of feedback switch and bus power switch circuit

3.2.2 Charge/discharge switch and communication capacitor power supply circuit

The circuit schematic diagram of the charge/discharge switch and communication capacitor power supply part in the CD1005 chip is shown inFigure 3.3, where: CHG_EN is the internal signal for controlling the charge switch tube, and DCHG_EN is the internal signal for controlling the discharge switch tube. Q1 is the charge switch tube, which is a PMOS tube with a nominal withstand voltage of 40V; Q2 is the control tube for controlling the charge switch,

is an NMOS tube with a nominal withstand voltage of 60V; Q3 is the discharge switch tube, which is an NMOS tube with a nominal withstand voltage of 60V; D1 and D2 are diodes with a nominal withstand voltage of 40V, and D3 is a diode with a nominal withstand voltage of 50V.

The nominal resistance of R1 is 2MΩ, the nominal resistance of R2 is 2.6MΩ, the nominal resistance of R3 is 25KΩ, and the nominal resistance of R4 is 501Ω.

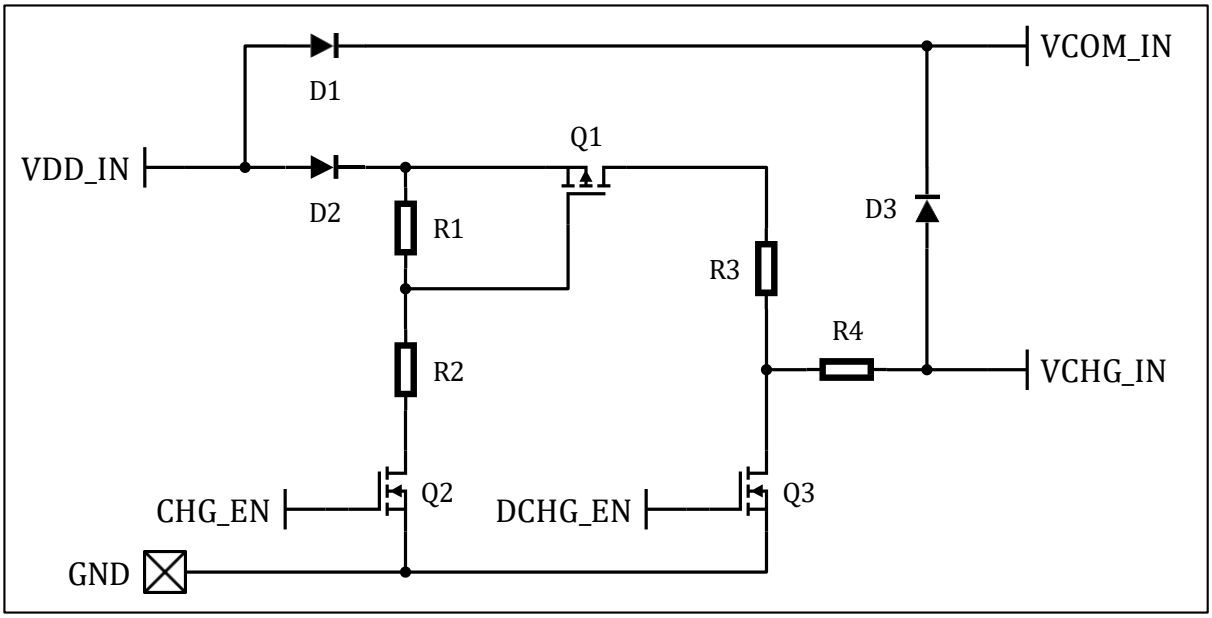

Figure 3.3 Schematic diagram of charge/discharge switch and communication capacitor power supply circuit

4 Communication

This section introduces the communication method of CD1005, including sending instructions from the host computer to CD1005 and feedback from CD1005 to the host computer.

The timing of the communication function is based on the internal clock control of CD1005. For the description of the clock, see 7 On-chip Clock, for the definition of the related instructions, see Appendix 2 Instruction Definition, and for the definition of the configuration area, see Appendix 1.1 Definition of Configuration Area.

4.1 Sending instructions from the host computer to CD1005

In this document, "host computer" refers to all devices that supply power to CD1005 through the peripheral circuit A and B buses and send instructions, including but not limited to detonators, module testers, three-code binding instruments, packaging testers, etc.

Among the A and B buses, there is always a bus voltage of VA-B and the other bus voltage is 0V. The voltage difference of VA-B is always maintained between the two buses to ensure the stability of power supply. The process of the host computer switching the voltage of one of the A and B buses from VA-B to 0V and the voltage of the other bus from 0V to VA-B is called bus polarity switching. The host computer sends instructions to CD1005 by switching the polarity of the A and B buses according to a certain rule.

The level change of A and B buses can refer toFigure 4.1。

In this document, for the sake of simplicity, all descriptions of bus polarity are only explained with the bus with the initial level of VA-B as an example. The bus polarity when its level is VA-B (that is, the other bus is 0V at the same time) is called high level, and vice versa is called low level; the switching process from VA-B to 0V (that is, the other bus switches from 0V to VA-B at the same time) is called falling edge, and vice versa is called rising edge.

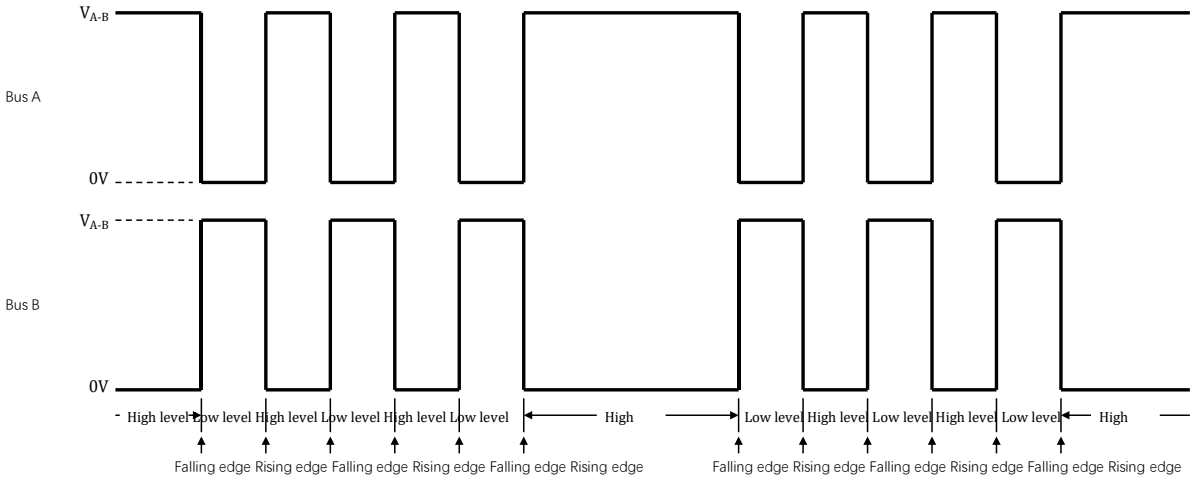

Figure 4.1 Example of A and B bus levels

4.1.1 Related configuration area fields

Among the fields in the configuration area, the communication clock frequency division and bit end character threshold are related to the function of the host computer sending instructions to CD1005. For specific descriptions, seeTable 4.1。

Table 4.1 Description of configuration area fields related to the host computer sending instructions to CD1005

Symbol	Description	Unit	Fixed value
T_{comm}	Communication clock cycle	μs	$2^{(4\text{-}SET1[7:6])}\times T_{osc}$
$T_{bit\ end\ thresh.}$	Bit end character judgment threshold time	μs	$(18+2\times SET1[3:0])\times T_{comm}$

4.1.2 Definition of data bit

The host computer switches the bus polarity, then waits for a certain time and switches the bus polarity again, and then waits for a certain time, which is called a cycle. Multiple cycles are performed continuously, and then the bus polarity is kept at a high level for a period of time, and a data bit is sent to CD1005. The number of cycles in the data bit determines whether the data bit is 0 or 1.

For the specific timing definition of the data bits, seeTable 4.2 andFigure 4.2. The figure only takes the bus with the initial level of VA-B as an example, and the level of the other bus is opposite.

Table 4.2 Timing definition of the host computer sending data bits to CD1005

Symbol	Description	Unit	Minimum value	Maximum value
T_{low}	Time to maintain a low level in the data bit sending cycle	μs	20	--
T_{high}	Time to maintain a high level in the data bit sending cycle	μs	20	$T_{bit\ end\ thresh.}$
$T_{bit\ end}$	Time to maintain a high level at the end of the bit	μs	$T_{bit\ end\ thresh.}$	--
T_{period}	Time from one rising edge to the next rising edge	μs	--	$255\times T_{comm}$
N_{one}	Number of cycles representing data bit 1	individual	2	4
N_{zero}	Number of cycles representing data bit 0	individual	5	--

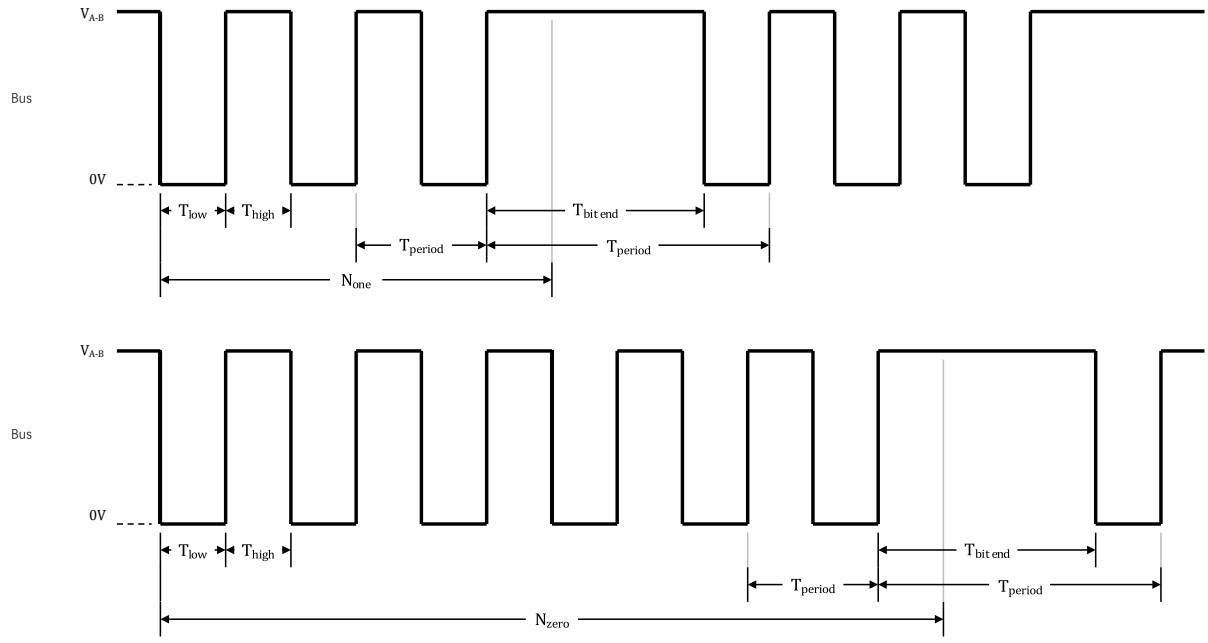

Figure 4.2 Timing diagram of the host computer sending data bit 1 or 0 to CD1005

4.1.3 Definition of square wave

In some instructions, after the instruction data is transmitted, the host computer is also required to send a square wave to CD1005. These square waves play two roles. One is to provide an accurate time reference for the CD1005 chip so that the CD1005 can calibrate the internal clock on site to achieve accurate delay time. The other is to serve as a synchronous timing signal so that multiple CD1005 chips can provide feedback in a unified timing when networking. The former is called calibration square wave, and the latter is called feedback square wave.

After the command data is sent, the host computer waits for a certain period of time before starting to send square waves. The host computer switches the bus polarity, waits for a certain period of time, switches the bus polarity again, and then waits for a certain period of time before sending a square wave to CD1005. According to the command requirements, it may be necessary to send multiple such square waves continuously.

The specific timing definition of the square wave is shown inTable 4.3 andFigure 4.3. The figure only takes the bus with the initial level of VA-B as an example, and the level of the other bus is opposite. It should be noted that the time from the last rising edge of the instruction to the first rising edge of the square wave also needs to follow Tperiod, which is the upper limit of the time from one rising edge to the next rising edge.

Table 4.3 Timing definition of the host computer sending square waves to CD1005

Symbol	Description	Unit	Minimum value	Maximum value
$T_{interval}$	Time from the last rising edge of the instruction to the first falling edge of the square wave	μs	$T_{bit\ end\ thresh.}$	--
T_{width}	Waiting time between two switching polarities in the square wave	μs	20	--
T_{period}	Time from one rising edge to the next rising edge	μs	--	$255\times T_{comm}$

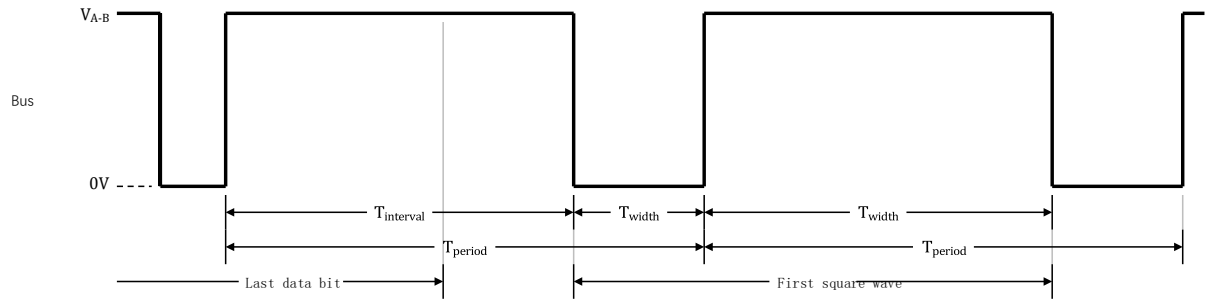

Figure 4.3 Timing diagram of the host computer sending square waves to CD1005

4.1.4 Instruction content

Continuously sending 8 data bits constitutes 1 byte, and continuously sending several bytes constitutes an instruction.

The instruction consists of 1 or 2 instruction code bytes, 0 or several data bytes, and 1 CRC check byte. A square wave may be required after some instructions. For the format definition of specific instructions, please refer to Appendix 2 Instruction Definition.

The CRC check byte in the instruction is the result of CRC calculation for the entire instruction including the instruction code byte and all data bytes. The check adopts the classic CRC-8 method, that is, the CRC check method with a width of 8, a generating polynomial of $X^8 + X^2 + X + 1$, and a check result initial value of 0x00. If the CRC check in the received instruction is incorrect, CD1005 will not perform any operation and will not give any feedback.

Here, we take several typical instructions as examples to explain the instruction format:

Take the "number value read detonator information" instruction as an example, the instruction format is "instruction code + number value + parameter + CRC + square wave × (N + 2) × 8", where the instruction code is 0xA2, and N is the number of bytes of information specified by the parameter field. We assume that the number value is 0x1234, and the information to be read is the number value, delay value, and status register. The signal sequence to be sent by the host computer is shown in Table 4.4 As shown.

Table 4.4 Example of the "Read detonator information by number value" instruction

Sequence	Operation	Hexadecimal	Binary data bit
1	Send instruction code byte	0xA2	1010 0010
2	Send data byte 1	0x12	0001 0010
3	Send data byte 2	0x34	0011 0100
4	Send data byte 3	0xC4	1100 0100
5	Send CRC check byte	0x58	0101 1000
6	Send 64 feedback square waves continuously		

Taking the "delayed calibration" instruction as an example, the instruction format is "instruction code + CRC + square wave × 129", where the instruction code is 0x2E 2D. Then the signal sequence to be sent by the host computer is as follows Table 4.5 As shown.

Table 4.5 Example of "Delayed calibration" instruction

Sequence	Operation	Hexadecimal	Binary data bit
1	Send instruction code byte 1	0x2E	0010 1110
2	Send instruction code byte 2	0x2D	0010 1101
3	Send CRC check byte	0xBB	1011 1011
4	Continuously send 129 calibration square waves		

4.1.5 Receiving and processing instructions

While the host computer sends instructions through the bus, CD1005 will also synchronously identify and process the polarity changes on the bus. When the instruction is sent, CD1005 will judge the end of the instruction according to a certain timing and start to execute the operation required by the instruction.

For instructions that do not require square waves, CD1005 always uses the last bit end character of the instruction as the basis for judging the end of the instruction. The timing description of CD1005 ending instruction recognition and starting instruction execution is shown inTable 4.6 andFigure 4.4. In the figure, only the bus with the initial level of VA-B is used as an example. The level of the other bus is opposite.

Table 4.6 Timing description of CD1005 starting instruction execution

Symbol	Description	Unit	Fixed value
$T_{exec.}$	Time from the last edge of the instruction to the start of CD1005 execution	μs	$4\times T_{osc}+T_{bit\ end\ thresh.}+T_{comm}$

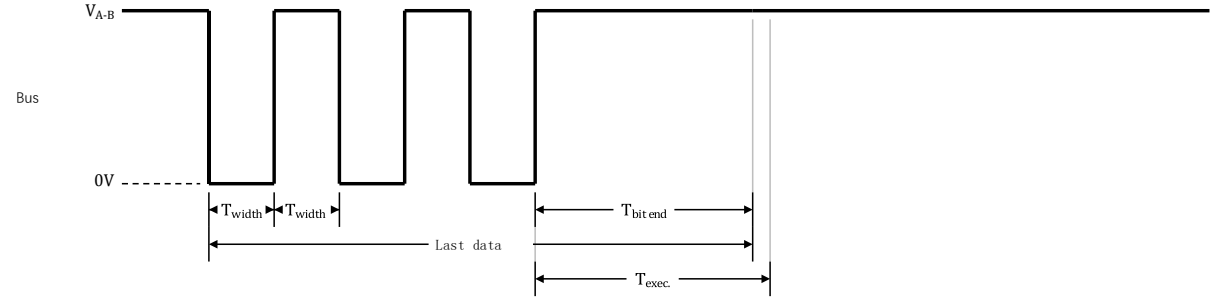

Figure 4.4 Timing diagram of CD1005 starting instruction execution

For instructions that require square waves, the criteria for CD1005 to determine the end of the instruction part and start execution are the same as those for instructions that do not require square waves. However, CD1005 will not completely end the reception of the current instruction and start waiting for the next instruction until it determines that the square wave has ended. Therefore, the interval between the last edge of the square wave and the next instruction must be greater than the determination time. The timing description of CD1005 determining the end of the square wave is shown inTable 4.7 andFigure 4.5. In the figure, only the bus with the initial level of VA-B is used as an example. The level of the other bus is opposite.

Table 4.7 Timing description of CD1005 determining the end of the square wave

Symbol	Description	Unit	Fixed value
$T_{cw\ end}$	Time from the last edge of the square wave to the time when CD1005 determines that it has ended	μs	$4\times T_{osc}+256\times T_{comm}$

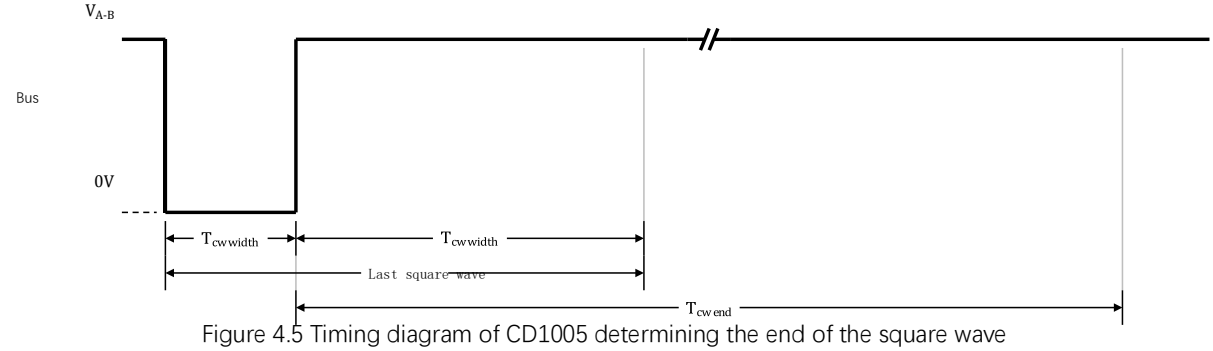

Figure 4.5 Timing diagram of CD1005 determining the end of the square wave

4.2 Feedback from CD1005 to the Host Computer

CD1005 also needs to send feedback to the host computer through the bus. This feedback is sometimes for transmitting data to the host computer, sometimes for reporting the time to complete an action to the host computer, or for feedback of other information.

CD1005 feedback is achieved by opening the feedback switch between VDD and GND, forming a path between VDD and GND, thereby increasing the current consumed by the chip. CD1005 opens the feedback switch, waits for a period of time, and then closes it, thereby causing the bus current to increase first and then return to the initial state. This is called a feedback pulse. The host computer receives this feedback by monitoring the change in current on the bus.

Feedback can be divided into three situations according to the form of feedback, namely: direct feedback, square wave feedback, and feedback after detonation. The following is an introduction one by one.

4.2.1 Related configuration area fields

Among the fields in the configuration area, the three fields of communication clock division, feedback start time, and feedback duration are related to the function of CD1005 to provide feedback to the host computer. For details, seeTable 4.8。

Table 4.8 Description of fields in the configuration area related to CD1005's feedback to the host computer

Symbol	Description	Unit	Fixed value
T_{comm}	Communication clock cycle	μs	$2^{(4-SET1[7:6])}\times T_{osc}$
$T_{fb.\,start}$	Start time of feedback pulse in square wave feedback	μs	$5\times T_{osc}+(20+SET2[7:4])\times T_{comm}$
$T_{fb.\,width}$	Duration of feedback pulse	μs	$(19+SET2[3:0])\times T_{comm}$

4.2.2 Direct feedback

Direct feedback refers to sending only one feedback pulse and does not require the host computer to provide a synchronous signal feedback. This feedback is usually used to inform the host computer when a certain action is completed. For example, in the "master code charge/discharge" instruction, a direct feedback indicates that charging is completed; for example, in the "write master code" instruction, a direct feedback indicates that writing is completed.

The waveform of direct feedback is shown inFigure 4.6The bus level shown in the figure is only based on the bus with an initial level of VA-B as an example, and the other bus level is the opposite.

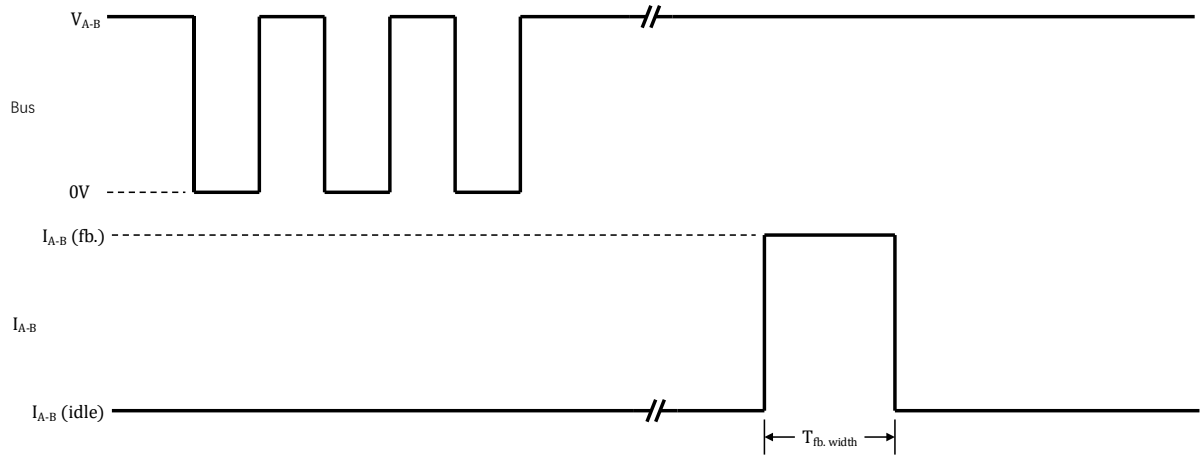

Figure 4.6 Direct feedback waveform diagram

4.2.3 Square wave feedback

Square wave feedback is the most commonly used feedback method. This feedback method requires the host computer to send a square wave for synchronization. This feedback is usually used to transmit data to the host computer, or to coordinate all CD1005 chips to feedback according to a certain rule under networking conditions. For example, in the "number value read detonator information" instruction, CD1005 transmits the information field specified in the instruction to the host computer through square wave feedback; for another example, in the "get verification status shot by shot" instruction, all CD1005 in the network feedback the status of the flag bit specified in the instruction in the corresponding square wave according to their respective number values.

For the waveform and timing description of square wave feedback, seeFigure 4.7. The bus level shown in the figure only takes the bus with the initial level of VA-B as an example, and the other bus level is opposite. For the timing of the bus square wave itself, see 4.1.3 Definition of square wave.

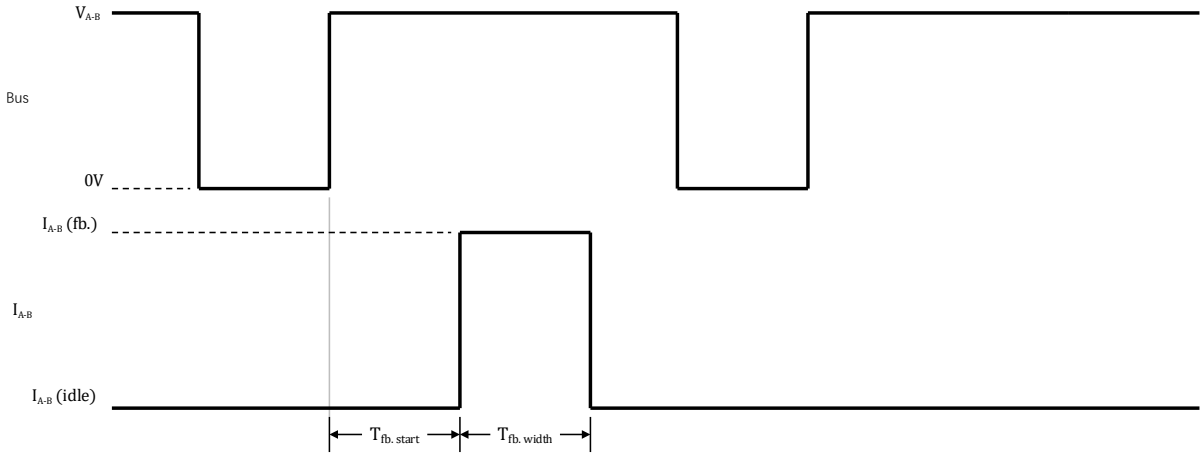

Figure 4.7 Square wave feedback waveform diagram

4.2.4 Feedback after detonation

In order to facilitate the detection of whether the ignition function is normal, CD1005 is designed with feedback after detonation. That is, after the ignition switch is turned on, it detects whether the power on the energy storage capacitor is lower than the voltage corresponding to the charging 3V gear. If it is lower than the voltage corresponding to the charging 3V gear, six feedback pulses are issued; if it is higher than the voltage corresponding to the charging 3V gear, no feedback is given. That is, if the host computer detects feedback after detonation, it means that the voltage on the energy storage capacitor is released, that is, the detonation function is normal.

For detailed description of feedback after detonation, see 13.4 Detonation process.

4.3 Recommended Communication Format

This chapter introduces the definition of the communication format between CD1005 and the host computer, but the specific communication format can be flexibly adjusted within the allowable range, including the format of the data bit and square wave sent by the host computer and the configuration inside the chip.

This section introduces three recommended communication formats, which are respectively compatible with the CD1005 chip in the default state, common typical networking conditions, and extreme networking conditions with large bus parasitic resistance and capacitance.

4.3.1 Communication format for chip default state

When the host computer sends data bit 0, it sends 6 cycles, in which the waiting time between each switching polarity is 140μs, 110μs, 130μs, 120μs, 130μs, 120μs, 130μs, 120μs, 130μs, 120μs, 130μs, 120μs, 130μs, and 130μs. After the last edge of each bit, keep the bus polarity unchanged for 480μs.

When the host computer sends data bit 1, it sends 3 cycles, and the waiting time between each polarity switch is
140μs, 110μs, 130μs, 120μs, and 130μs respectively. After the last edge of each bit, the bus polarity remains unchanged for 480μs. When the host computer sends a square wave, after the last edge of the instruction, the bus polarity remains unchanged for 700μs, and then starts to send
square waves. In each square wave, the bus polarity is switched first, wait for 500μs, switch the bus polarity again, and wait for 700μs. In the configuration area of CD1005, the communication clock division is configured as 0x3, the bit end character threshold is configured as 0x2, the feedback
start time is configured as 0x0, and the feedback duration is configured as 0x0

4.3.2 Communication format for typical scenarios

When the host computer sends data bit 0, it sends 6 cycles, and the waiting time between each polarity switch is 220μs, 180μs, 220μs, 200μs, 220μs, 200μs, 220μs, 200μs, 220μs, 200μs, 220μs, and 220μs. After the last edge of each bit, the bus polarity remains unchanged for 560μs.
When the host computer sends data bit 1, it sends 3 cycles, and the waiting time between each polarity switch is
220μs、180μs、220μs、200μs、220μs, After the last edge of each, keep the bus polarity unchanged for 560 μ s. When the upper computer sends a square wave, after the last edge of the instruction, keep the bus polarity unchanged for 1700 μ s, and then start
Send square waves. In each square wave, first switch the bus polarity and wait for 500 μ s, then switch the bus polarity again and wait for 1700 μ s.
In the configuration area of CD1005, the communication clock division is configured as 0x2, the bit end character threshold is configured as 0x0, the feedback start time is configured as 0x0, and the feedback duration is configured as 0x0

4.3.3 Communication format for extreme scenarios

5 Data Storage

5.1 Definition of Each Storage Field

The definition of each storage field in CD1005 is shown inTable 5.1。

In the storage fields defined inTable 5.1 , the three fields commonly used at the detonation site, namely, the number value, the delay value, and the short spare area, are collectively referred to as the site value.

Table 5.1 Definition of each storage field in CD1005

Field name	Abbreviation	Length	Description
Primary code	PID	8	Code used for addressing of A1 type single-shot communication command, can choose detonator UID or shell code
Secondary code	SID	13	CD1005 only stores unused codes, can choose detonator UID or shell code
Detonation password	PWD	8	Detonation password, only allows detonation after verification, cannot be read
Number value	INDEX	2	Code used for addressing of A2 type single-shot communication command, also used for command of calling out one by one
Delay value	DELAY	2	Used to set the delay time with millisecond accuracy
Short spare area	BAK_S	2	Short spare area that can be read by single shot or scanning, can store various information required by customers
Version number	REV	2	Used to store the version number of the chip or module
Calibration value	CAL	3	Used to calibrate the low voltage power supply, reference voltage source, clock frequency, etc.
Configuration area	SET	3	Used to configure the various functions of CD1005
Spare area	BAK	13	Spare area that can be read out by single shot, can store various information required by customers
Lock flag	LOCK	2	Used to record whether CD1005 is locked by hardware
Status	STATUS	2	Various flags used to record the working status of CD1005

5.2 On-Chip Data Register

5.2.1 General register

CD1005 has 13 bytes of general registers inside, called GPR0~GPR12, which are used as buffers when reading and writing various data fields. Among them, GPR11~GPR12 are also used as 16-bit general counters.

5.2.2 Special registers

CD1005 has multiple groups of special registers inside, which are used to store the information required for the normal operation of the chip and temporary variables in the field networking process. They are 3-byte calibration value register, 3-byte configuration area register, 2-byte number value register, 2-byte extension value register, and 2-byte status register.

5.3 On-Chip Non-Volatile Memory

CD1005 has an on-chip non-volatile memory (NVM) for storing the calibration value, configuration area, version number, primary code, secondary code, detonation password, spare area, number value, extension value, short spare area and other information of the detonator, as well as other configuration information necessary for the chip to work.

Among them, the number value, extension value, calibration value, and configuration area fields have both dedicated registers and corresponding NVM

storage. When describing them, this document will specify whether it is registers or NVM that are read and written. For these fields, during reset loading, if the calibration value has been written, CD1005 will replace the value of the calibration value register with the calibration value NVM, otherwise the default value is used; if the configuration area has been written, CD1005 will replace the value of the configuration area register with the configuration area NVM, otherwise the default value is used; if both the calibration value and the configuration area have been written, CD1005 will replace the values of the number value register and the extension value register with the values of the number value NVM and the extension value NVM, otherwise the default value is used.

For the relevant parameters of the NVM integrated in CD1005, see Table 5.2。

Table 5.2 Main parameters of the NVM on the CD1005 chip

Parameter definition	Unit	Typical value	Maximum value
Storage capacity	Byte	128	
Number of pages	individual	8	
page size	Byte	16	
Addressing mode (when reading)		Byte addressing	
Addressing mode (when writing)		Page addressing	
Access time (the time required to read a byte)	μs	$2\times T_{osc}$	
Write time (the time required to write a page)	ms	18	31
Power consumption (when in standby)	μA	<1	15
Power consumption (when writing)	μA	700	1,800
Power consumption (when reading)	μA	100	300

5.4 Methods for Reading and Writing Data

5.4.1 Reading data

The host computer can read the data in the dedicated register or NVM of CD1005 by sending specific instructions to CD1005.

These commands include:

- "Master code reads detonator information" command, which can read out the number value register, extension value register, short spare area, version number, calibration value register, and status register
- "Master code reads secondary code" command, which can read out the secondary code
- "Master code reads spare area" command, which can read out the spare area
- "Number value reads detonator information" command, which can read out the number value register, extension value register, short spare area, version number, calibration value register, and status register
- "Number value reads secondary code" command, which can read out the secondary code
- "Number value reads spare area" command, which can read out the spare area
- "Scan" command, which can read out the master code, number value register, extension value register, short spare area, version number, calibration value register, and status register
- "Read secondary code" command, which can read out the secondary code, which is not available in the locked state
- The "read field value" command can read the number value NVM, extension value NVM, short spare area, which is not available in the locked state.
- The "read spare area" command can read the spare area, which is not available in the locked state.
- The "read version number and configuration area" command can read the version number and configuration area registers, which is not available in the locked state.
- The "read version number and configuration area NVM" command can read the version number and configuration area NVM, which is not available in the locked state.

The specific definition of the above commands is shown in **Appendix 2 Command Definition**。

5.4.2 Write data

The host computer sends specific commands to CD1005 to modify the data in the dedicated register or NVM in CD1005. When writing NVM, CD1005 will give a direct feedback after the writing is completed to inform the host computer that the writing is completed.

These commands include:

- "Master code write site value" command, can modify the number value register, delay value register
- "Number value write site value" command, can modify the delay value register
- "Set configuration area" command, can modify the configuration area register
- "Write master code" command, can modify the master code, not available in locked state
- "Write detonation password" command, can modify the detonation password, not available in locked state
- "Write secondary code" command, can modify the secondary code, not available in locked state
- "Write field value" command, can modify the number value register and NVM, extension value register and NVM, short spare area, not available in locked state
- "Write spare area" command, can modify the spare area, not available in locked state
- "Write version number and configuration area" command, can modify the version number, configuration area register and NVM, not available in locked state

The specific definition of the above commands is shown in**Appendix 2 Command Definition**。

6 Reset Process

6.1 Reset

6.1.1 Power-on reset

When the AB bus power supply voltage reaches 6.5V, CD1005 starts power-on reset, and the reset ends after a period of time. The specific timing of this reset process is shown inTable 6.1 andFigure 6.1。

Table 6.1 CD1005 power-on reset timing description

Symbol	Description	Unit	Maximum value
T_{reset}	Time from reset start to reset end	μs	$5{,}000\times T_{osc}$

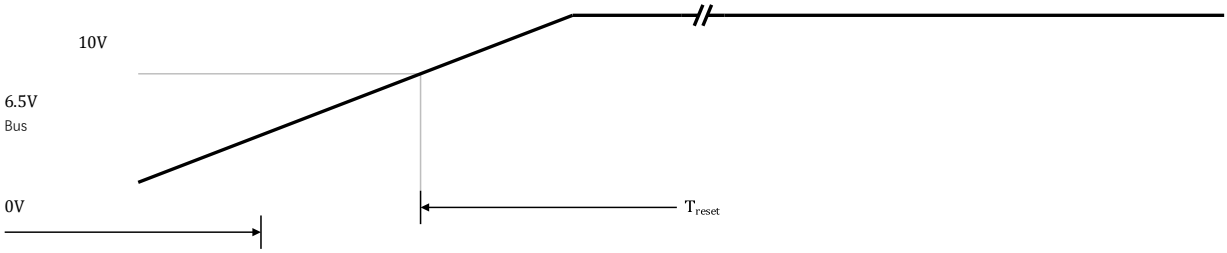

Figure 6.1 CD1005 power-on reset timing diagram

6.1.2 Software reset

There are two instructions that can make CD1005 actively trigger reset, they are "software reset" instruction and "detonation" instruction. Among them, the "software reset" instruction is an instruction that does not require a square wave, and will immediately start to execute reset when the instruction is received; the "detonation" instruction is an instruction that requires a square wave. If the detonation conditions in CD1005 are not met, the reset will be executed after the square wave ends. For the specific timing of the above two instructions triggering software reset, seeTable 6.2、 Figure 6.2 andFigure 6.3。

Table 6.2 CD1005 software reset timing description

Symbol	Description	Unit	Maximum value
$T_{exec.}$	Time from the last edge of the instruction to the start of CD1005 execution	μs	$4\times T_{osc}+T_{bit\ end\ thresh.}+T_{comm}$
$T_{cw\ end}$	Time from the last edge of the square wave to the end of CD1005	μs	$4\times T_{osc}+256\times T_{comm}$
T_{reset}	Time from reset start to reset end	μs	$5{,}000\times T_{osc}$

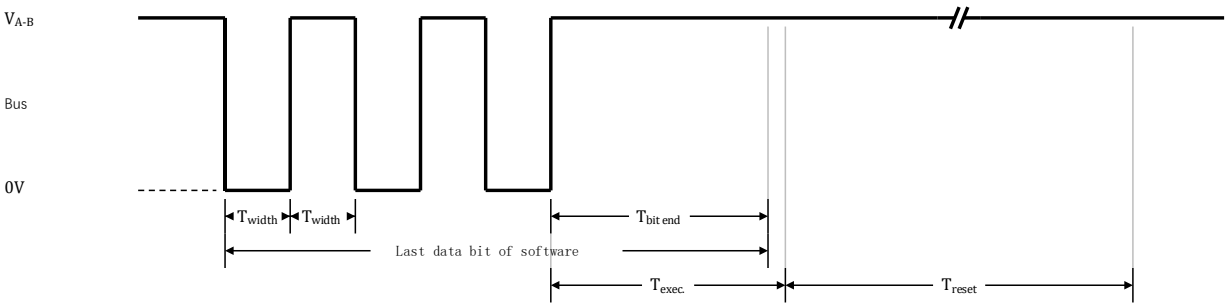

Figure 6.2 Timing diagram of software reset triggered by the "software reset" instruction

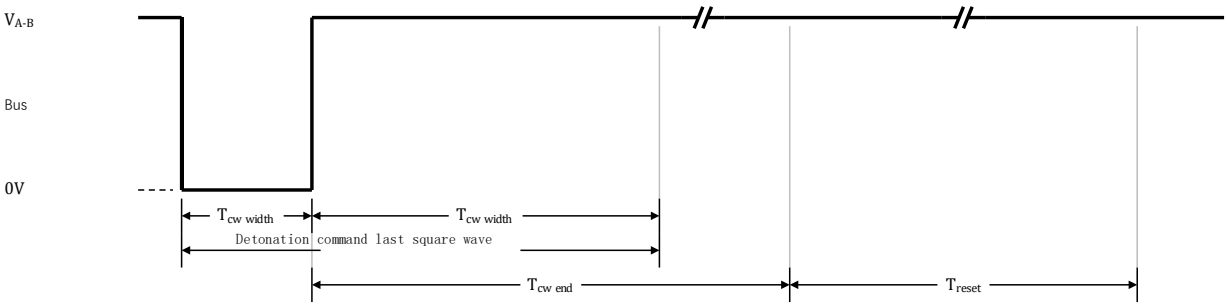

Figure 6.3 Timing diagram of software reset triggered by the "detonation" instruction

6.2 Data Loading

After the reset is completed, CD1005 will execute the data loading process, during which data is loaded from NVM and the default values of the relevant special registers are replaced by the data loaded from NVM.

The order of CD1005 loading data is: 2-byte calibration value write flag, 3-byte calibration value, 1-byte calibration value CRC and check, 2-byte configuration area write flag, 3-byte configuration area, 1-byte configuration area CRC and check, 2-byte hardware lock flag, 2-byte number value NVM, 2-byte extension value NVM.

The rules for CD1005 to perform data loading are as follows:

Only when the calibration value write flag has been written and the calibration value CRC is correct, CD1005 will replace the default value of the calibration value register with the loaded calibration value, and set the calibration value write flag bit in the status register to 1.

Only when the configuration area write flag has been written and the configuration area CRC is correct, CD1005 will replace the default value of the configuration area register with the loaded configuration area, and set the configuration area write flag bit in the status register to 1.

Only when the calibration value write flag bit and the configuration area write flag bit in the status register are both 1, CD1005 will set the hardware lock state according to the hardware lock flag in NVM, and replace the default values of the number value register and the delay value register with the loaded number value and delay value.

If the calibration value write flag bit and the configuration area write flag bit in the status register are not all 1 when the data loading process is completed, CD1005 will not enter the standby state, but will wait for a certain period of time before automatically loading again. During the waiting process, only the "set test pin" command can be recognized. When receiving this command, CD1005 will stop automatically reloading.

For the timing description of the data loading process, seeTable 6.3。

Table 6.3 CD1005 data loading timing description

Symbol	Description	Unit	Maximum value
$T_{load\ byte}$	Time to load one byte of data	μs	$2\times T_{osc}$
$T_{calc.\ CRC}$	Time to check one byte of CRC	μs	$8\times T_{osc}$
T_{load}	Total time for the complete data loading process	μs	$18\times T_{load\ byte}+8\times T_{calc.\ CRC}$
T_{reload}	Time between two automatic reloads	μs	$205{,}104\times T_{osc}$

6.3 Polarity Identification

After the data loading is completed, CD1005 will perform the bus polarity identification process. During this process, CD1005 will count. If the bus polarity changes, it will re-count until the bus polarity remains unchanged for 513×Tcomm. At this time, the polarity identification process ends, and CD1005 will regard the bus polarity at this time as the standby polarity, and identify the bus signal based on this. After the polarity identification process is completed, CD1005 enters the standby state.

For the specific definition of the above flags, see **Appendix 1.2 Definition of Status Register**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

7 On-Chip Clock

7.1 Brief Description of On-Chip Clock

CD1005 has an internal clock oscillator module to provide clock for digital control logic.
The clock module generates a base clock signal with a target frequency of 200KHz, and then passes through a set of clock dividers to generate a lower frequency clock signal for communication logic and delay logic. These two lower frequency clock signals are called communication clock and delay clock respectively.

7.2 Configuration of Clock Division

The SET1[7:6] bits in the configuration area are used to configure the frequency division of the communication clock. By modifying these two bits in the configuration area register, the frequency of the communication clock can be set to 1/16, 1/8, 1/4 or 1/2 of the clock oscillator frequency, and the corresponding communication clock period becomes 16, 8, 4, or 2 times the clock oscillator period.
The SET1[5:4] bits in the configuration area are used to configure the frequency division of the delayed clock. By modifying these two bits in the configuration area register, the frequency of the delayed clock can be set to 1/64, 1/32, 1/16 or 1/8 of the clock oscillator frequency, and the corresponding delayed clock period becomes 64, 32, 16, or 8 times the clock oscillator period.
It Should Be Noted That the Communication Clock Should Not Be Configured to a Frequency Slower Than the Delayed Clock Frequency, Otherwise It May Cause an Abnormal Error in the Execution of the Instruction.
The "Set Configuration Area" instruction and the "Write Version Number and Configuration Area" instruction can modify the above configuration area registers.

For the specific definition of the above configuration area, see **Appendix 1.1 Definition of Configuration Area**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

8 Lock Function

8.1 Lock Function

CD1005 provides a lock function. In the locked state, all C-class instructions cannot be executed, so that the data stored in the NVM cannot be modified.
The lock state is controlled by two bits in the status register, which are called the software lock flag bit and the hardware lock flag bit. When either of these two flag bits is 1, CD1005 is in the locked state.

8.1.1 Software Lock

Software lock is controlled by the configuration area. When the SET0[0] bit in the configuration area register is 1, the software lock flag bit is 1.
The value of this bit can be modified using the "Set Configuration Area" command and the "Write Version Number and Configuration Area" command. For chips that have not written to the configuration area, the default value of this bit is 1.

8.1.2 Hardware lock

Hardware lock is controlled by the hardware lock flag in NVM. For chips that have been written with configuration area and calibration values, if the lock command has been executed before, the hardware lock flag will change to 1 after reset and loading.
Use the "lock" command to write the hardware lock flag to NVM and change the hardware lock flag in the status register to 1.

8.2 Unlock Function

In the locked state, if you want to release the software lock, you should use the "set configuration area" command to set the SET0[0] bit in the configuration area register to 0 to release the software lock.
If the configuration area NVM has been written, when CD1005 is reset and loaded, the value in the configuration area NVM will replace the value in the configuration area register.
Hardware lock cannot be released.

For the specific definition of the above flags, see **Appendix 1.2 Definition of Status Register**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

9 Network Scanning Function

CD1005 is designed with a "scan" command, which can use the anti-collision mechanism to read out the master code of all networked CD1005 chips in sequence after the network is completed, and can choose to read out other information besides the master code. Using the "scan" command, users can check whether there are multiple or missing chips after networking.

9.1 Related Configuration Area Fields

Among the fields in the configuration area, the three fields of communication clock division, feedback start time, and feedback duration are related to the network scanning function. For details, seeTable 9.1。

Table 9.1 Description of fields in the configuration area related to the network scanning function

Symbol	Description	Unit	Fixed value
T_{comm}	Communication clock cycle	μs	$2^{(4\text{-SET1}[7:6])}\times T_{osc}$
$T_{fb.start}$	Start time of feedback pulse in square wave feedback	μs	$5\times T_{osc}+(20+SET2[7:4])\times T_{comm}$
$T_{fb.width}$	Duration of feedback pulse	μs	$(19+SET2[3:0])\times T_{comm}$

9.2 Scan Anti-Collision Mechanism

The core of the "scan" instruction is the anti-collision mechanism, which is based on the premise that the master codes of all CD1005 chips in the network are different.

When CD1005 receives the "scan" instruction, if the scan read flag is 0, it starts to feedback its own master code and other information specified by the parameters in the instruction.

At the same time, the host computer detects feedback in each square wave. If feedback is detected (that is, if a CD1005 feedbacks 1), the bus polarity is switched immediately. If the CD1005 that feeds back 0 (i.e. does not send out current feedback pulse) in this square wave detects that the bus polarity switches in advance, it means that there are other CD1005s feeding back in this square wave, and it will immediately exit the feedback of the "scan" instruction until the current instruction ends.

In this way, when the master code feedback in each "scan" instruction is completed, only the CD1005 with the largest master code number is still feeding back. When the chip has fed back all its data to be fed back (including the master code and other information), it will set its scan read flag to 1, so that the chip will no longer respond when it receives the "scan" instruction next time. Therefore, the host computer only needs to send the "scan" instruction continuously to read the master code and other information of all CD1005s in the network in the order of the master code numbers from large to small.

Scan anti-collision mechanism related timing and waveform illustrationTable 9.2 andFigure 9.1。

Table 9.2 Scan anti-collision mechanism timing description

Symbol	Description	Unit	Fixed value
T_{check}	Time from bus rising edge to polarity switching detection	μs	$(50+SET2[7:4]+SET2[3:0])\times T_{comm}$

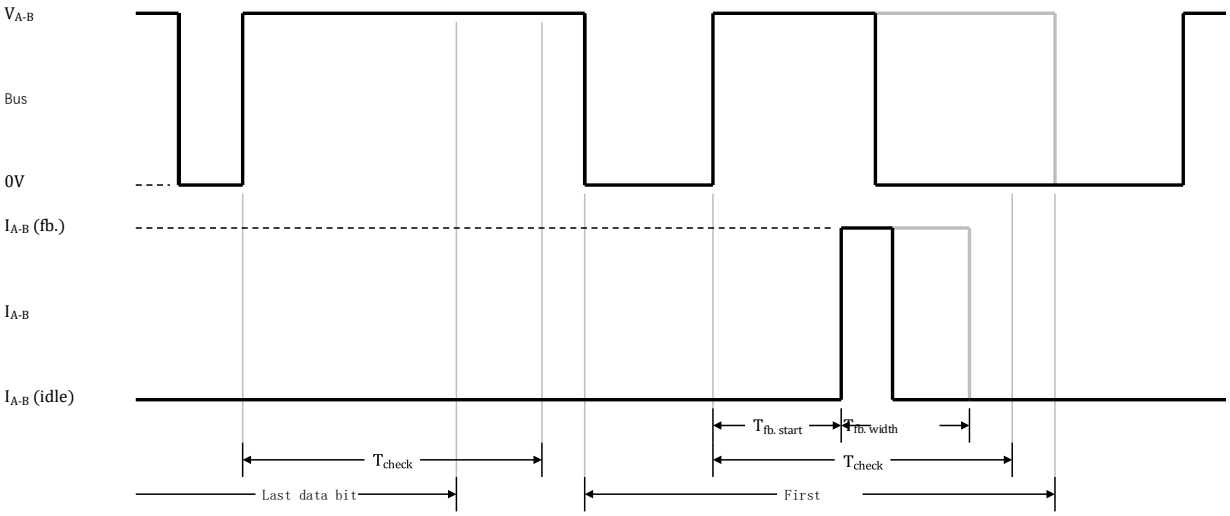

Figure 9.1 Scan anti-collision mechanism waveform illustration

9.3 Scan Instruction Parameter Description

There is a 1-byte parameter field in the "scan" command, which is used to specify other feedback information for CD1005 besides the main code, as well as whether to enable the automatic allocation of number values function. Its definition is shown in Table 9.3。

Table 9.3 "Scan" instruction parameter definition

Bit	Definition
[7]	1 Feedback number value register (2 bytes), 0 No feedback
[6]	1 Feedback delay value register (2 Byte), 0 No feedback
[5]	1 Short spare area feedback (2 bytes), 0 No feedback
[4]	1 Version number feedback (2 bytes), 0 No feedback
[3]	1 Feedback calibration value register (2 bytes), 0 No feedback
[2]	1 Feedback status register (2 bytes), 0 No feedback
[1]	Undefined
[0]	1 Enable automatic numbering function, 0 Disable automatic numbering function

9.3.1 Scan and read information selection

After CD1005 feedbacks the main code in the "Scan" command, it will continue to feedback the information specified in the parameters. This information is fed back in the order of Table 9.3 . After the feedback is completed, 1 byte CRC and end byte will also be fed back.

For example, if the parameter of a "scan" instruction is 0xC4, that is, bits [7], [6], and [2] are 1, then after receiving the instruction, CD1005 will sequentially feedback 8-byte master code, 2-byte number value register, 2-byte extension value register, 2-byte status register, 1-byte CRC, and 1-byte end byte.

9.3.2 Scan automatic number value assignment function

If bit [0] in the parameter of the "scan" instruction is 1, that is, the automatic numbering function is enabled, then when CD1005 receives the "scan" instruction, if the scan read flag is 0, it will accumulate a count; if a chip in a "scan" instruction fully feedbacks the master code, it will write this count value into its number value register. If the feedback number value register is also specified in this scan instruction, the feedback value is also the count value.

It should be noted that the counter that maintains this count value inside CD1005 is universal and will also be used in other instructions, so its value is uncertain. Therefore, to use this function, you need to send the "clear read" command first, which will clear the above counter, so that the count value when the "scan" command is sent later will start to accumulate from 1.

For the specific definition of the above flags, see **Appendix 1.2 Definition of Status Register**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

10 Detonation Password Management

10.1 Writing of Detonation Password

In the unlocked state, the host computer sends the "write detonation password" command to CD1005 to write the detonation password to the NVM of CD1005

The length of the detonation password field is 8 bytes.

After the writing is completed, CD1005 will give a direct feedback to inform the host computer that the writing is completed. The detonation password cannot be read after it is written, and cannot be modified in the locked state.

10.2 Detonation Password Verification

CD1005 can only be charged or detonated after the detonation password is verified, that is, when the detonation password verification pass flag in the status register is 1.

There are 3 instructions for detonation password verification, namely the "master code verification detonation password" instruction, the "number value verification detonation password" instruction, and the "verification detonation password" instruction.

For the "master code verification detonation password" instruction and the "number value verification detonation password" instruction, after receiving the instruction, CD1005 will first compare the master code or number value in the instruction. If the master code or number value in the instruction is consistent with the master code or number value register in the chip, CD1005 will further compare the detonation password in the instruction. If the detonation password in the instruction is consistent with the detonation password in the chip, CD1005 will set the detonation password verification pass flag in the status register to 1, and feedback 1 byte 0xAA in the square wave of the instruction; if the detonation password in the instruction is inconsistent with the detonation password in the chip, CD1005 will not modify the detonation password verification pass flag, and feedback 1 byte 0xFF in the square wave of the instruction.

For the "verify detonation password" instruction, after receiving the instruction, CD1005 will compare the detonation password in the instruction. If the detonation password in the instruction is consistent with the detonation password in the chip, CD1005 will set the detonation password verification pass flag in the status register to 1, and feedback 1 byte 0xAA in the square wave of the instruction; if the detonation password in the instruction is inconsistent with the detonation password in the chip, CD1005 will not modify the detonation password verification pass flag, and will not feedback in the square wave of the instruction.

For the specific definition of the above flags, see **Appendix 1.2 Definition of Status Register**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

11 Delay Time Control Function

11.1 Delay Value Setting

Delay value is a data field used to set the delay time with millisecond accuracy. The delay value actually used in CD1005 is stored in its delay value register. The delay value also has a corresponding NVM storage. When CD1005 is reset, if the calibration value and configuration area have been written to NVM, the data will be loaded from NVM to the delay value register, otherwise the default value of the delay value register, i.e. 65,535, will be used.

There are 3 instructions to set the delay value of CD1005, namely "Master code write field value" instruction, "Number value write field value" instruction, and "Write field value" instruction.

For the "Master code write field value" instruction, after receiving the instruction, CD1005 will first compare the master code in the instruction. If the master code in the instruction is consistent with the master code in the chip, CD1005 will write the number value and delay value in the instruction into the number value register and delay value register.

For the "write site value to number value" instruction, after receiving the instruction, CD1005 will first compare the number value in the instruction. If the number value in the instruction is consistent with the number value register in the chip, CD1005 will write the delay value in the instruction into the delay value register.

For the "write site value" instruction, after receiving the instruction, CD1005 will write the number value, site value and short spare area in the instruction into NVM, and write the number value and site value in the instruction into the number value register and the delay value register.

11.2 Delay Time Calibration

In order to ensure the accuracy of the delay time, CD1005 needs to calibrate the delay time at the detonation site. Only after the delay time calibration of CD1005, that is, when the delay calibration completion flag bit in the status register is 1, CD1005 can detonate.

The host computer sends the "delay calibration" command to calibrate the delay time. After receiving the command, CD1005 will record the number of delay clock cycles corresponding to the rising edge of the 1st square wave to the rising edge of the 129th square wave of the command. When the record is completed, CD1005 will set the delay calibration completion flag in the status register to 1.

It should be noted that the default value of the delay value register is 65,535. In order to prevent the failure to write the delay value and cause detonation refusal, when the delay value register is 65,535, CD1005 does not execute the delay calibration command. Therefore, when the delay calibration completion flag of CD1005 is not 1 during the pre-detonation inspection, it should be noted that the value of the delay value register should be confirmed.

It should also be noted that, because the delay time calibration mechanism is related to the delay clock division, when the delay clock division is modified (using the "Set Configuration Area" instruction or the "Write Version Number and Configuration Area" instruction, the delay clock division in the instruction is different from before), CD1005 will also set the delay calibration completion flag in the status register to 0.

For the specific definition of the above flags, see **Appendix 1.2 Definition of Status Register**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

12 Energy Storage Capacitor Charge/Discharge Control

CD1005 can charge/discharge the energy storage capacitor on the electronic detonator module. There are 3 instructions to control the charge/discharge of the energy storage capacitor, namely the "Master Code Charge/Discharge" instruction, the "Number Value Charge/Discharge" instruction and the "Charge/Discharge" instruction. Among them, the "Master Code Charge/Discharge" instruction and the "Number Value Charge/Discharge" instruction belong to Class A instructions, which are used to control a single CD1005 chip under networking conditions, and the "Charge/Discharge" instruction belongs to Class B instructions, which are used to control all networked CD1005 chips. The following are explained separately.

12.1 Class A Charge/discharge Instruction Description

There is a 1-byte parameter field in the "main code charge/discharge" command and the "number value charge/discharge" command, which is used to specify the charging gear or select the discharge function. Its definition is shown in Table 12.1。

Table 12.1 "Master code charge/discharge" instruction and "number value charge/discharge" instruction parameter definition

Bit	Definition
[7:4]	Undefined
[3:0]	Charging position, 1~9 3V, 5V, 10V, 12V, 14V, 16V, 18V, 20V, 22V, Others discharge

After receiving the instruction, CD1005 will first compare the master code or number value in the instruction. If the master code or number value in the instruction is consistent with the master code or number value register in the chip, CD1005 will charge/discharge according to the gear specified in the instruction parameter.

12.2 Description of Class B Charge/discharge Instructions

The "charge/discharge" command contains a 3-byte parameter field that specifies the upper and lower limits for matching delay values, the number of valid digits for matching serial numbers, the charging gear, or the selection of the discharge function. Its definition can be found in Table 12.2。

Table 12.2 "Charge/discharge" instruction parameter definition

Bit	Definition
[23:16]	Delay value matching interval lower limit L 0~255 Charge only when the delay value in the chip is greater than or equal to (L×256)
[15:8]	Delay value matching interval upper limit H 0~255 Charge only when the delay value in the chip is less than or equal to (H×256)
[7:4]	Number of digits matching the number value N 0~15 Charging is performed only when the high (16-N) bit of the number value in the chip is consistent with the high (16-N) bit of the number value in the instruction
[3:0]	Charging gear, 1~9 3V, 5V, 10V, 12V, 14V, 16V, 18V, 20V, 22V, the rest discharging

After receiving the instruction, CD1005 will first match the significant digit pairs according to the specified number value in the instruction parameters

Match the number values in the command and match the upper and lower limits of the delay values specified in the instruction parameters. If both the number value and the delay value match, CD1005 will charge/discharge according to the gear specified in the instruction parameters.
The number value matching mechanism can realize group charging to prevent all modules from charging too much at the same time, or for different types of modules in the same network that require different charging voltages.
The delay value matching mechanism can select different charging voltages according to different delay values, so as to more accurately match the ignition voltage of the charge head.

The following is a detailed description of the number value and delay value matching mechanism.

12.2.1 Number value matching mechanism

The [7:4] bits in the parameters of the "charge/discharge" instruction specify the number of bits N for the number value matching. At the same time, there is a number value field with a length of 2 bytes in the instruction.
When receiving this instruction, the CD1005 chip compares the high (16-N) bits of the number value in the instruction with the high (16-N) bits of the number value register in the chip. If they are the same, the match is passed; if they are not the same, the match is not passed.
For example, if the number value in a "charge/discharge" instruction is 0x01 FF, and the parameter [7:4] bit is 0x8, then the CD1005 chip whose number value register is between 0x01 00 and 0x01 FF passes the match; if two CD1005 chips receive the instruction, and the number value registers are 0x00 FF and 0x01 00 respectively, the former fails to match, while the latter passes.

12.2.2 Delay value matching mechanism

The [23:16] bits in the parameter of the "charge/discharge" instruction specify the lower limit L of the delay value matching interval, and the [15:8] bits specify the upper limit H of the delay value matching interval.
When receiving the instruction, the CD1005 chip compares the upper 8 bits of the delay value register in the chip with L and H in the instruction. If the upper 8 bits of the delay value register are greater than or equal to L and less than or equal to H, the match passes, otherwise the match fails.
For example, if the parameter [23:16] bits in a "charge/discharge" instruction are 0x04 and [15:8] bits are 0x07, then the CD1005 chip matching between the delay value register of 0x04 00 (i.e., delay time 1.024s) and 0x07 FF (i.e., delay time 2.047s) passes; if two CD1005 chips receive the instruction, and the delay value registers are 0x03 E8 (i.e., delay time 1s) and 0x07 D0 (i.e., delay time 2s), the former fails to match, but the latter passes.

12.3 Control of Charging Voltage of Energy Storage Capacitors

After CD1005 receives the "master code charge/discharge" instruction, "number value charge/discharge" instruction or "charge/discharge" instruction and compares or matches, if the parameter in the instruction specifies the charging gear, CD1005 will start charging the energy storage capacitor.
After starting to charge, CD1005 will periodically check whether the voltage of the energy storage capacitor has reached the target voltage corresponding to the specified charging voltage gear. If it has reached the target voltage, it will stop charging, otherwise it will continue to charge. After charging reaches the target voltage, it will continue to periodically check the voltage of the energy storage capacitor. If it is found that the target voltage has not been reached, it will restart charging to maintain the voltage of the energy storage capacitor stable and fluctuate around the target voltage.

The timing diagram of CD1005's function of controlling the charging voltage of the energy storage capacitor and the related electrical characteristic parameters are shown in Table 12.3 and Figure 12.1。

Table 12.3 Electrical characteristics of the energy storage capacitor voltage control function

Symbol	Parameter definition	Unit	Minimum value	Typical value	Maximum value
V_{VCHG} (target)	Target voltage corresponding to the charging gear (3~5V gear)	V	Gear voltage ±0.2		
V_{VCHG} (target)	Target voltage corresponding to the charging gear (10~22V gear)	V	Gear voltage ±2.5%		
ΔV_{VCHG}	Fluctuation range of VVCHG after full charge (CVCHG≥33μF)	mV	--	--	50
I_{VCHG} (peak)	Peak value of VCHG pin output current during charging	mA	--	--	1.5
T_{cycle}	Check the cycle of the energy storage capacitor voltage	μs	$32\times T_{osc}$		

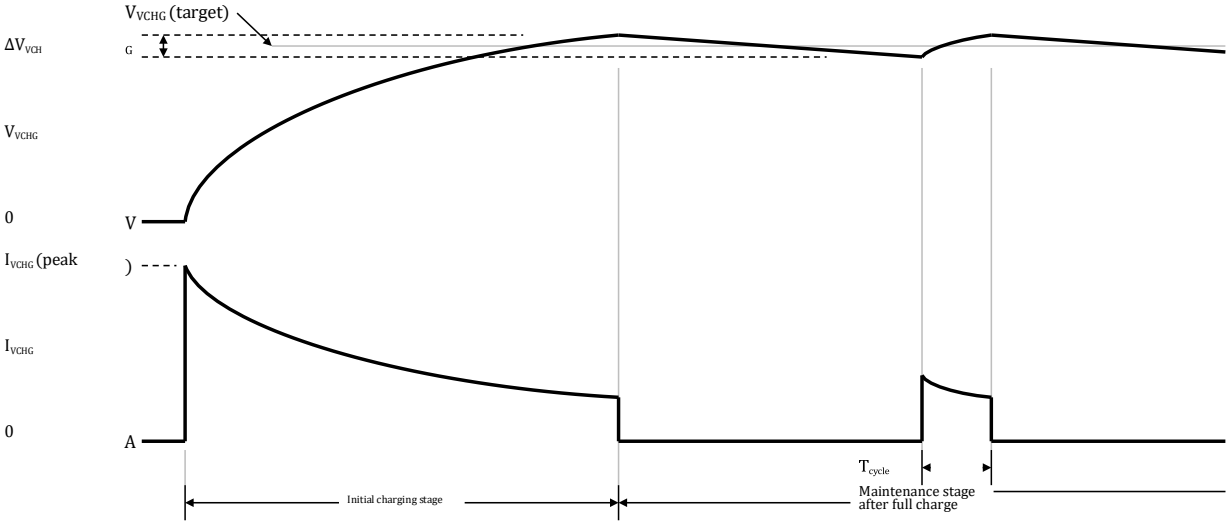

Figure 12.1 Voltage and current diagram of the energy storage capacitor voltage control function

12.4 Energy Storage Capacitor Discharge Control

After CD1005 receives the "master code charge/discharge" instruction, "number value charge/discharge" instruction or "charge/discharge" instruction and compares or matches, if the parameters in the instruction specify discharge, CD1005 will start to discharge the energy storage capacitor.

For the relevant electrical characteristics of the discharge function, see Table 12.4。

Table 12.4 Electrical characteristics of energy storage capacitor discharge function

Symbol	Parameter definition	Unit	Minimum value	Typical value	Maximum value
I_{VCHG} (dchg.)	Current of VCHG during discharge (VVCHG=20V)	mA	--	--	15

12.5 Description of Flag Bits Related to Charging Function

There are 2 flag bits in the status register related to the charge/discharge function, namely the once fully charged flag bit and the currently fully charged flag bit. The logic is: when the CD1005 chip is reset, the once fully charged flag bit and the currently fully charged flag bit are both 0. When receiving the charge/discharge command and the comparison or matching passes, if the charging gear is specified in the parameter, the current full charge flag is set to 0; if the discharge is specified in the parameter, the once fully charged flag and the current fully charged flag are set to 0. When fully charged, the once fully charged flag and the current fully charged flag are set to 1.

For the specific definition of the above flags, see **Appendix 1.2 Definition of Status Register**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

13 Detonation Control

13.1 Detonation Conditions and Their Inspection Methods

13.1.1 Detonation conditions

Only when the detonation password verification pass flag, the once fully charged flag, and the extended calibration completion flag in the status register are all 1, CD1005 determines that the detonation conditions are met.

Only when the detonation conditions are met, executing the detonation command will cause CD1005 to enter the extension process and the detonation process. When the detonation conditions are not met, executing the detonation command will cause the CD1005 software to reset.

13.1.2 Method for checking the detonation conditions and other status bits

There are 3 instructions that can check the 3 flag bits involved in the detonation conditions, namely the "Get all verification status" instruction, the "Get verification status shot by shot" instruction and the "Detonation" instruction.

Among them, the "Get all verification status" instruction and the "Get verification status shot by shot" instruction can not only check the 3 flag bits involved in the detonation conditions, but also check the remaining flag bits in the status register STATUS0.

1) "Get All Verification Status" Instruction

The host computer sends the "Get all verification status" instruction to quickly check whether the specified flag bits in the status register STATUS0 of all networked CD1005 chips are all 1.

In this instruction, there is a parameter field with a length of 1 byte, which is used to specify which flag bits need to be checked. Its definition is shown in Table 13.1。

Table 13.1 "Get all verification status" command parameter definition

Bit	Definition
[7]	Calibration value write flag, 1 check, 0 do not check
[6]	Configuration area write flag, 1 check, 0 do not check
[5]	Detonation password verification passed flag, 1 check, 0 do not check
[4]	Fully charged flag, 1 check, 0 do not check
[3]	Deferred calibration completed flag, 1 check, 0 do not check
[2]	Currently fully charged flag, 1 check, 0 do not check
[1]	Resistance open circuit check passed flag, 1 check, 0 do not check
[0]	Capacitor open circuit check passed flag, 1 check, 0 do not check

If the flag bits specified in the instruction to be checked are not all 1, CD1005 will feedback 0xFF in the square wave of the instruction; if the flag bits specified to be checked are all 1, CD1005 will not feedback. All networked CD1005 chips will feedback at the same time, so you only need to send a very short square wave to get the flag bit status of all networked CD1005 chips.

It should be noted that if no flag bit is specified in the instruction parameter, CD1005 will not feedback.

2) "Get Verification Status Shot by Shot" Instruction

The host computer sends the "Get verification status shot by shot" instruction to check whether the flag bit specified in the status register STATUS0 of each networked CD1005 chip is 1.

In this instruction, there is a 2-byte number value offset field, which is used to determine the square wave corresponding to each CD1005 chip. For each CD1005 chip, the (number value register - number value offset) the square wave of this instruction is its corresponding square wave.

In this instruction, there is a parameter field with a length of 1 byte, which is used to specify which flag bits need to be checked. Its definition is consistent with the parameters of the "Get All Verification Status" instruction, see Table 13.1。

If the flag bits specified in the instruction to be checked are all 1, CD1005 will feedback 1 in the corresponding square wave; if the flag bits specified to be checked are not all 1, CD1005 will not feedback. All networked CD1005 chips will feedback in their corresponding square waves, so that the flag bit status of each networked CD1005 chip can be obtained.

It should be noted that if no flag bit is specified in the instruction parameter, CD1005 will fixedly feedback 1 in its corresponding square wave, and then this instruction can play the role of network status check.

It should also be noted that to use this instruction, it is necessary to ensure that the number values of all networked CD1005 chips are different, and it is best to number them continuously.

3) "Detonation" instruction

The host computer sends the "detonation" instruction to check whether the detonation conditions of each networked CD1005 chip are met. If the detonation conditions are met, CD1005 will feedback 1 in the (number value register) square wave of the instruction; if

the detonation conditions are not met, CD1005 will not feedback.

This function is used to confirm that each CD1005 chip has received the detonation instruction and meets the detonation conditions at the last moment before the start of the extension process.

13.2 Ignition Switch and Its Control

The ignition switch is controlled by the FIRE pin, and the FIRE pin is controlled by a 5-bit internal signal, namely FE[4:0]. These 5 signals are separated from each other in space and will not flip at the same time logically. The FIRE pin will output a high level only when these five signals are 1, 0, 1, 0, 1, respectively. Otherwise, the FIRE pin will be pulled down to the ground by the logic circuit. Therefore, even if the external interference causes the weakly driven on-chip digital signal to be changed by mistake, it is impossible for the FIRE pin to output a high level. At the same time, on the basis of the pull-down of the logic circuit, the FIRE pin is also equipped with a pull-down resistor to play a double insurance role.

The relevant characteristics of the NMOS ignition switch are shown in Table 13.2, and the schematic diagram of its control structure is shown in Figure 13.1。

Table 13.2 Electrical characteristics of the NMOS ignition switch control structure

Symbol	Parameter definition	Unit	Minimum value	Typical value	Maximum value
R_{PD}	Pull-down resistor value	kΩ	70.8	101.1	131.4
V_{OH}	High-level output voltage (IFIRE<1mA)	V	VLDO-0.4	VLDO	--
V_{OL}	Low-level output voltage (IFIRE<1mA)	V	--	0	0.3

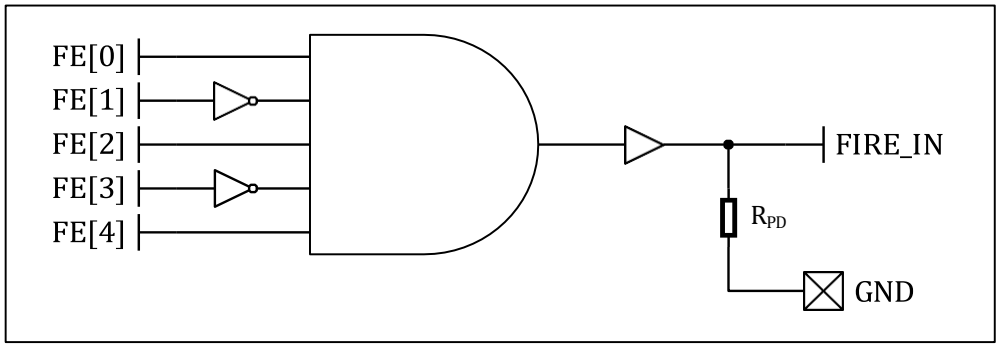

Figure 13.1 Schematic diagram of the control structure of the NMOS ignition switch

13.3 Entering the Delay and Delay Process

When the detonation conditions are met, sending the "detonation" command will cause the CD1005 to enter the delay state. The timing of entering the delay state varies depending on whether the parameter of the "detonation" command is 0, and is explained separately in this section.

13.3.1 Related configuration area fields

In the fields of the configuration area, the three fields of communication clock division, delay clock division, and bit end character threshold are related to the function of entering the delay state. For specific descriptions, see Table 13.3。

Table 13.3 Description of configuration area fields related to the delay process

Symbol	Description	Unit	Fixed value
T_{comm}	Communication clock cycle	μs	$2^{(4\text{-SET1[7:6]})} \times T_{osc}$
T_{timer}	Delay timer cycle	μs	$2^{(6\text{-SET1[5:4]})} \times T_{osc}$
$T_{bit\ end\ thresh.}$	Bit end character judgment threshold time	μs	$(18+2\times SET1[3:0]) \times T_{comm}$

13.3.2 Parameter is 0

If the parameter of the "detonation" command is 0, CD1005 will calculate the number of delay timer cycles corresponding to the delay value after receiving the detonation command, and then enter the delay state. After the delay ends, it will start to execute the detonation and post-detonation actions. During the delay process, CD1005 will turn on the feedback switch to isolate the interference from the bus.

The timing description of the process from receiving the "detonation" command to the end of the delay is shown in Table 13.4 and Figure 13.2, Figure 13.2 The bus levels shown in are only for the bus with the initial level of VA-B as an example, and the other bus level is the opposite.

Table 13.4 Delay process timing description when the "detonation" command parameter is 0

Symbol	Description	Unit	Minimum value	Maximum value
$T_{exec.}$	The time when the command starts to execute	μs	$T_{bit\ end\ thresh.}+T_{comm}$	
$T_{calc.\ d.}$	The time taken to calculate the delay time	μs	$30\times T_{osc}+T_{comm}$	$30\times T_{osc}+T_{timer}$
T_{delay} (ideal)	Ideal delay time	μs	$\lceil(\text{delay value}\times 1{,}000)/\text{Ttimer}\rceil\times\text{Ttimer}$	
T_{delay}	Delay time	μs	T_{delay} (ideal)-T_{timer}	T_{delay} (ideal)

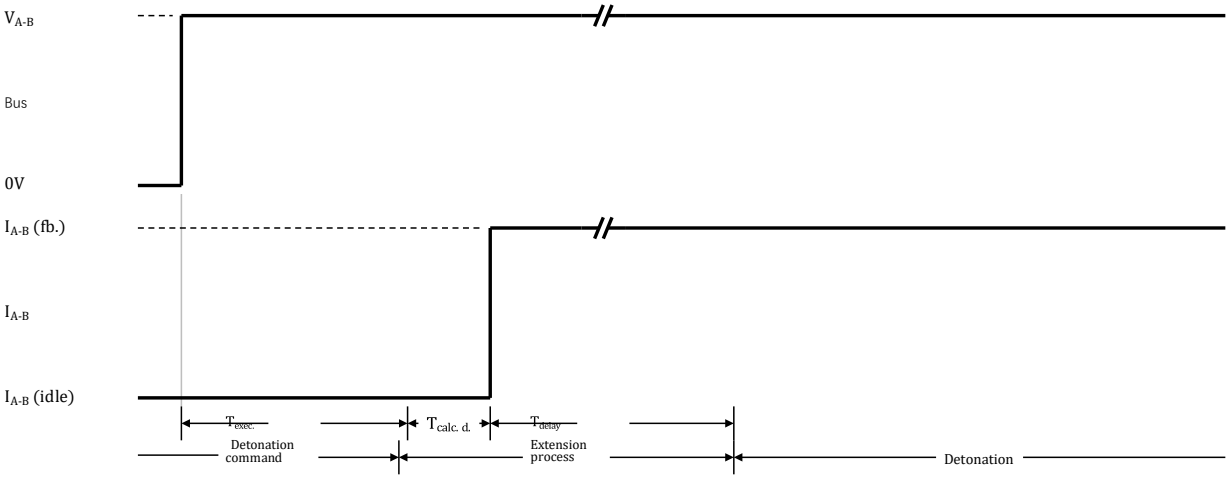

Figure 13.2 Delay process waveform when the parameter of the "detonation" command is 0

13.3.3 Parameter is not 0

If the parameter of the "detonation" command is not 0, CD1005 will calculate the countdown time before delay corresponding to the parameter after receiving the detonation command, and then count down before delay. After the countdown ends, it calculates the number of delay timer cycles corresponding to the delay value, and then enters the delay state. After the delay ends, it starts to execute the detonation and post-detonation actions. During the delay process, CD1005 will open the feedback switch to isolate the interference from the bus.

The timing description of the process from receiving the "detonation" command to the end of the delay is shown in Table 13.5 and Figure 13.3, Figure 13.3 The bus levels shown in are only for the bus with the initial level of VA-B as an example, and the other bus level is the opposite.

Table 13.5 Timing of the delay process when the "detonation" instruction parameter is not 0

Symbol	Description	Unit	Minimum value	Maximum value
$T_{exec.}$	The time when the command starts to execute	μs	$T_{bit\ end\ thresh.}+T_{comm}$	
$T_{calc.\ c.}$	The time taken to calculate the delay time	μs	$28\times T_{osc}+T_{comm}$	$28\times T_{osc}+T_{timer}$
$T_{ctd.}$ (ideal)	Ideal countdown time before delay	μs	$\lceil(\text{parameter}\times 256{,}000)/\text{Ttimer}\rceil\times\text{Ttimer}$	
$T_{ctd.}$	Countdown time before delay	μs	$T_{ctd.}$ (ideal)-T_{timer}	$T_{ctd.}$ (ideal)
$T_{calc.\ d.}$	The time taken to calculate the delay time	μs	$29\times T_{osc}$	
T_{delay} (ideal)	Ideal delay time	μs	$\lceil(\text{delay value}\times 1{,}000)/\text{Ttimer}\rceil\times\text{Ttimer}$	
T_{delay}	Delay time	μs	T_{delay} (ideal)-T_{timer}	T_{delay} (ideal)

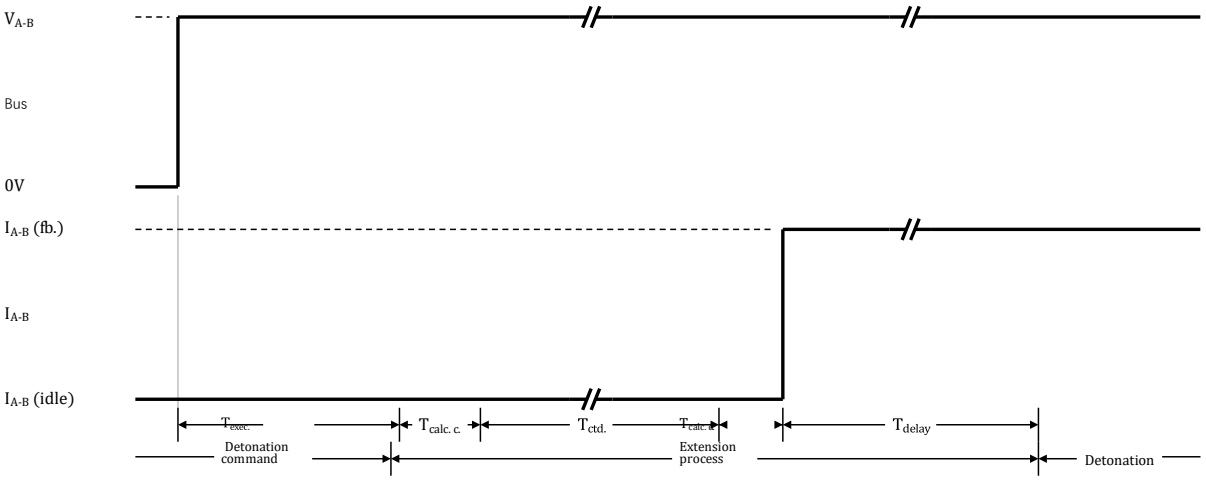

Figure 13.3 Waveform of the delay process when the "detonation" instruction parameter is not 0

13.4 Detonation Process

After the delay is over, CD1005 starts to flip the NMOS ignition switch control signal bit by bit after a certain interval,

After all 5-bit control signals are flipped, the NMOS ignition switch control pin FIRE becomes high level.

In order to facilitate the detection of whether the ignition function is normal, CD1005 is designed with post-detonation feedback. That is, after the ignition switch is turned on, CD1005 starts to detect the voltage of the VCHG pin. If the voltage of the VCHG pin is lower than the voltage corresponding to the charging 3V gear, six feedback pulses are issued; if it is higher than the voltage corresponding to the charging 3V gear, no feedback is performed. That is, if the host computer detects the post-detonation feedback, it means that the voltage on the energy storage capacitor is released, that is, the detonation function is normal.

After the post-detonation feedback ends, wait for a period of time, and CD1005 automatically performs software reset.

13.4.1 Timing description

For the timing description of the process from the end of delay to automatic reset after detonation, see Table 13.6 and Figure 13.4。

Table 13.6 Timing description of detonation process

Symbol	Description	Unit	Fixed value
T_{nmos}	Interval time from the end of delay to NMOS action	μs	$9\times T_{osc}$
T_{fire}	Time from NMOS action to the start of feedback after detonation	μs	$1{,}212\times T_{osc} - T_{pmos\ advance}$
$T_{fb.\ interval}$	Interval time of feedback pulses	μs	$96\times T_{osc}$
$T_{fb.\ width}$	Duration of feedback pulse	μs	$32\times T_{osc}$
T_{reset}	Time from the 6th feedback pulse to automatic reset	μs	$16\times T_{osc}$

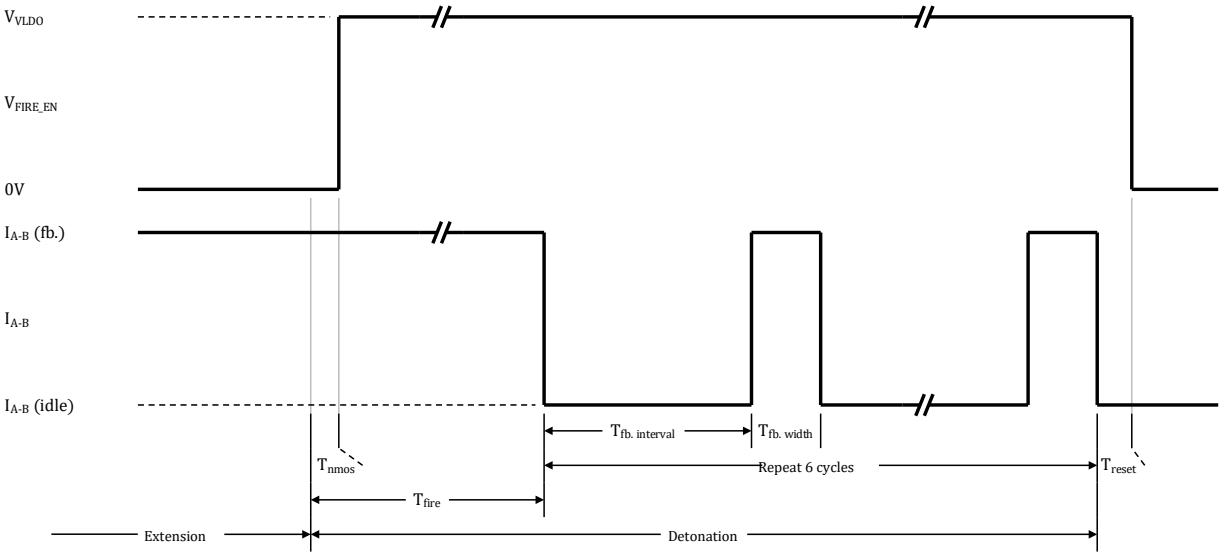

Figure 13.4 Waveform diagram of detonation process

For the specific definition of the above configuration area, see **Appendix 1.1 Definition of Configuration Area**。

For the specific definition of the above flags, see **Appendix 1.2 Definition of Status Register**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

14 Energy Storage Capacitor Open Circuit Detection Function

14.1 Energy Storage Capacitor Open Circuit Detection Method

CD1005 has the function of detecting the open circuit of energy storage capacitor. The detection method is to charge the energy storage capacitor through the energy storage capacitor charging function and check the energy storage capacitor voltage in a short time. If the voltage of the energy storage capacitor rises to the corresponding gear in a short time, the energy storage capacitor is judged to be open circuit, otherwise the energy storage capacitor is judged to be normal.

14.2 Instructions for Controlling the Open Circuit Detection Function of Energy Storage Capacitor

There are 3 instructions that can use the open circuit detection function of energy storage capacitor, namely the "master code check capacitor open circuit" instruction, the "number value check capacitor open circuit" instruction, and the "check capacitor open circuit" instruction. Among them, the "master code check capacitor open circuit" instruction and the "number value check capacitor open circuit" instruction belong to Class A instructions, which are used to control a single CD1005 chip under networking conditions, and the "check capacitor open circuit" instruction belongs to Class B instructions, which are used to control all networked CD1005 chips.

For the "master code check capacitor open circuit" instruction and the "number value check capacitor open circuit" instruction, after receiving the instruction, CD1005 will first compare the master code or number value in the instruction. If the master code or number value in the instruction is consistent with the master code or number value register in the chip, the comparison is passed, otherwise the comparison fails.

This instruction has a 1-byte parameter field, which is used to specify the timing of ending the check and selecting the charging position. For its definition, see Table 14.1。

Table 14.1 Parameter definitions of the "Master code check capacitor open circuit" instruction and the "Number value check capacitor open circuit" instruction

Bit	Definition
[7:4]	Undefined
[3:1]	Timing of ending the check T 0~7 end the check and start feedback at the (T×2+1)th square wave rising edge
[0]	Charging position, 0 3V position, 1 5V position

For the "Check capacitor open circuit" instruction, after receiving the instruction, CD1005 will first match the number value in the instruction according to the number value specified in the instruction parameter to the valid digits. The matching method is the same as the number value matching method of the "Charge/Discharge" instruction. For details, see **12.2.1 Number value matching mechanism**。

This instruction has a 1-byte parameter field, which is used to specify the number of valid bits of the matching number value, the timing of ending the check, and the selection of the charging gear. The definition is as follows Table 14.2。

Table 14.2 "Check capacitor open circuit" instruction parameter definition

Bit	Definition
[7:4]	Number of digits matching the number value N 0~15 The high (16-N) bit of the number value in the chip is consistent with the high (16-N) bit of the number value in the instruction before the check is performed
[3:1]	Timing of ending the check T 0~7 end the check and start feedback at the (T×2+1)th square wave rising edge
[0]	Charging position, 0 3V position, 1 5V position

For these 3 instructions for checking capacitor open circuit, CD1005 receives the instruction and compares or matches the main code or number value, and then starts the capacitor open circuit detection. The specific logic is as follows:

When receiving the instruction, set the capacitor open circuit checked flag bit and the capacitor open circuit check passed flag bit to 0. Then check whether the status of the charging switch and the discharging switch are off and on respectively. If so, turn off the discharging switch, turn on the charging switch, start charging the energy storage capacitor, and turn on the energy storage capacitor voltage comparator and set the charging gear according to the parameters in the instruction.

When the rising edge of the (T×2+1)th square wave is received, turn off the charging switch, turn on the discharging switch, and set the capacitor open circuit checked flag to 1. If the energy storage capacitor voltage has not been detected to reach the specified gear before, set the capacitor open circuit check passed flag to 1.

After the inspection is completed, in the (T×2+1)th to 24th square waves, if the capacitor open circuit check passed flag is 1, then alternately feedback 1 and 0; otherwise, feedback 1 in each square wave.

14.3 Flags Related to the Energy Storage Capacitor Open Circuit Detection Function

There are 2 flags in the status register related to the energy storage capacitor open circuit detection function, namely, capacitor open circuit detected Check flag and capacitor open circuit check pass flag. The meanings of different combinations of these two flags are shown in Table 14.3。

Table 14.3 Meanings of flags related to energy storage capacitor open circuit detection function

Capacitor open circuit has been Check flag	Capacitor open circuit check Pass flag	Meaning
0	0	Energy storage capacitor open circuit check has not been performed after reset
0	1	This situation does not exist
1	0	Energy storage capacitor open circuit check has been performed, and the check did not pass
1	1	Energy storage capacitor open circuit check has been performed, and the check passed

For the specific definition of the above flags, see **Appendix 1.2 Definition of Status Register**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

15 Drug Head Resistor Open Circuit Detection Function

15.1 Drug Head Resistor Open Circuit Detection Method

CD1005 has the function of detecting drug head resistor open circuit. Its detection method is to turn on NMOS The ignition switch is turned on, and then a current is output to the positive end of the drug head resistor through a current limiting circuit. After a certain period of time, the voltage at the positive end of the drug head resistor is checked. If the voltage is greater than a certain threshold at this time, the drug head resistor is judged to be open circuit, otherwise the drug head resistor is judged to be normal.

15.2 Instructions for Controlling the Drug Head Resistor Open Circuit Detection Function

There are 3 instructions that can use the drug head resistor open circuit detection function, namely the "master code check resistor open circuit" instruction, the "number value check resistor open circuit" instruction, and the "check resistor open circuit" instruction. Among them, the "master code check resistor open circuit" instruction and the "number value check resistor open circuit" instruction belong to Class A instructions, which are used to control a single CD1005 chip under networking conditions, and the "check resistor open circuit" instruction belongs to Class B instructions, which are used to control all networked CD1005 chips.

For the "master code check resistor open circuit" and "number value check resistor open circuit" instructions, after receiving the instruction, CD1005 will first compare the master code or number value in the instruction. If the master code or number value in the instruction is consistent with the master code or number value register in the chip, the comparison passes, otherwise the comparison fails.

This instruction has a 1-byte parameter field, which is used to specify the timing of ending the check and selecting the charging position. For its definition, see Table 15.1。

Table 15.1 Parameter definition of "Master code check resistor open circuit" instruction and "Number value check resistor open circuit" instruction

Bit	Definition
[7:4]	Undefined
[3:0]	Timing of ending the check T 0~15 End the check and start feedback at the rising edge of the (T×8+9)th square wave

For the "Check resistor open circuit" instruction, after receiving the instruction, CD1005 will first match the number value in the instruction according to the number value specified in the instruction parameter to match the valid digits. The matching method is the same as the number value matching method of the "Charge/Discharge" instruction. For details, see **12.2.1 Number value matching mechanism**。

This instruction has a 1-byte parameter field, which is used to specify the number of valid bits of the matching number value, the timing of ending the check, and the selection of the charging gear. The definition is as follows Table 15.2。

Table 15.2 Parameter definition of "Check resistor open circuit" instruction

Bit	Definition
[7:4]	Number of digits matching the number value N 0~15 The high (16-N) bit of the number value in the chip is consistent with the high (16-N) bit of the number value in the instruction before the check is performed
[3:0]	Timing of ending the check T 0~15 End the check and start feedback at the rising edge of the (T×8+9)th square wave

For these 3 instructions for checking resistor open circuit, CD1005 starts the resistor open circuit detection after receiving the instruction and comparing or matching the master code or number value. The specific logic is as follows:
Upon receiving the command, check whether the states of the charging switch and the discharging switch are off and on respectively. If so, turn on the energy storage capacitor voltage comparator and set the charging position to 3V.
When the falling edge of the first square wave is received, set the resistance open circuit checked flag and the resistance open circuit check passed flag to 0. Then check whether the states of the charging switch and the discharging switch are off and on respectively, and whether the energy storage capacitor voltage is less than the target voltage corresponding to the 3V charging position. If so, turn off the discharging switch and turn on the NMOS ignition switch. After the NMOS ignition switch is turned on, start the resistance measurement circuit, start to output current to the positive end of the drug head resistor through the current limiting output, and monitor the voltage of the positive end of the drug head resistor in real time. If the voltage at the positive end of the resistor reaches the threshold voltage specified by the "Resistance Measurement Reference Voltage Selection" field in the chip configuration area register, or the voltage of the energy storage capacitor reaches the target voltage corresponding to the 3V charging gear, the NMOS ignition switch is immediately turned off, the resistance measurement circuit is turned off, the discharge switch is turned on, and the energy storage capacitor voltage comparator is turned off.
When the rising edge of the (T×8+9)th square wave is received, the NMOS ignition switch is turned off, the resistance measurement circuit is turned off, the discharge switch is turned on, the energy storage capacitor voltage comparator is turned off, and the resistance open circuit has been checked flag is set to 1. If the resistance measurement circuit is still working at this time, the resistance open circuit check passed flag is set to 1.
In the (T×8+9)~(T×8+16)th square wave, if the resistance open circuit check passed flag is 1, then feedback 1 byte 0xAA; otherwise feedback 1 byte 0xFF.

15.3 Flags Related to the Energy Storage Capacitor Open Circuit Detection Function

There are two flag bits in the status register that are related to the open circuit detection function of the drug head resistance, namely, the resistance open circuit has been detected Check the flag bit and open circuit resistance check. The different combinations of these two flag bits represent the following meanings Table 15.3。

Table 15.3 Meanings of flags related to the open circuit detection function of the drug head resistor

Open circuit detection of the resistor Check flag	Open circuit detection of the resistor Pass flag	Meaning
0	0	Open circuit detection of the drug head resistor has not been performed after reset
0	1	This situation does not exist
1	0	Open circuit detection of the drug head resistor has been performed, and the check has not passed
1	1	Open circuit detection of the drug head resistor has been performed, and the check has passed

It should be noted that: because the positive end of the drug head resistor is also connected to the positive end of the energy storage capacitor, the current output by the resistance measurement circuit will also be shunted to charge the energy storage capacitor. Therefore, the T value needs to be large enough to make the voltage at the positive end of the drug head resistor reach the threshold when the drug head resistor is open.

For the specific definition of the above flags, see **Appendix 1.2 Definition of Status Register**. For the specific definition of the above instructions, see **Appendix 2 Command Definition**。

Appendix 1 Definition of Configuration Area and Status Register

Appendix 1.1 Definition of Configuration Area

Byte	Bit	Default value	Definition
SET0	[7:5]	0	Reserved
	[4]	1	Check resistor reference voltage selection, 0 0.3V, 1 0.5V
	[3:1]	5	Reserved
	[0]	1	Software lock, 0 allow the use of C-type instructions, 1 prohibit the use of C-type instructions
SET1	[7:6]	3	Communication clock division, 0 1/16, 1 1/8, 2 1/4, 3 1/2
	[5:4]	3	Delay clock division, 0 1/64, 1 1/32, 2 1/16, 3 1/8
	[3:0]	2	Bit end character threshold, threshold (communication clock number) = 18+2×SET1[3:0]
SET2	[7:4]	0	Feedback start time, time (number of communication clocks) = 20 + SET2 [7: 4]
	[3:0]	0	Feedback duration, time (number of communication clocks) = 19 + SET2 [3: 0]

Appendix 1.2 Definition of Status Register

Byte	Bit	Default value	Definition
STATUS0	[7]	0	Calibration value write flag, 1 written, 0 not written
	[6]	0	Configuration area write flag, 1 written, 0 not written
	[5]	0	Detonation password verification passed flag, 1 passed, 0 not passed
	[4]	0	Once fully charged flag, 1 Once fully charged, 0 Never fully charged
	[3]	0	Delayed calibration completed flag, 1 completed, 0 not completed
	[2]	0	Currently fully charged flag, 1 Currently fully charged, 0 Currently not fully charged
	[1]	0	Resistance open circuit check passed flag, 1 passed, 0 not passed
	[0]	0	Capacitor open circuit check passed flag, 1 passed, 0 not passed
STATUS1	[7]	1	Software lock flag, 1 locked, 0 unlocked
	[6]	0	Hardware lock flag, 1 locked, 0 unlocked
	[5]	0	Resistance open circuit checked flag, 1 checked, 0 unchecked
	[4]	0	Capacitor open circuit checked flag, 1 checked, 0 unchecked
	[3]	0	Scan read flag, 1 do not respond to scan command, 0 respond to scan command
	[2]	1	Charge switch, 1 charge switch closed, 0 charge switch open
	[1]	1	Discharge switch, 1 discharge switch open, 0 discharge switch closed
	[0]	1	Even parity, so that there must be an even number of 1s in the status byte

Appendix 2 Command Definition

Appendix 2.1 A1 Class Instructions (Instructions addressed by master code)

Instruction name	Master code write field value		
Instruction code	0xEC	Instruction content	Instruction code + master code + number value + extension value + CRC + square wave × 8
Content description	The length of the master code field is 8 bytes; the length of the number value field is 2 bytes; the length of the extension value field is 2 bytes.		
Instruction function	When the master code is correct and the CRC check passes: set the scan read flag to 1; store the number value and extension value fields in the instruction into the number value and extension value registers. When the master code is correct and the CRC check passes: the square wave feedback is 0xAA in the square wave.		

Instruction name	Master code reads detonator information		
Instruction code	0xEF	Instruction content	Instruction code + master code + parameter + CRC + square wave × (N + 2) × 8
Content description	The length of the master code field is 8 bytes; the length of the parameter field is 1 byte, defined as follows: N is the number of bytes of information specified by the parameter field.		
Instruction function	The main code is correct, after the CRC check is passed: according to the order of each bit in the parameter from high to low, the information specified in the parameter field is fed back in the square wave; after the information feedback is completed, the scan read flag is set to 1, and 1 byte CRC and 1 byte 0x80 are continued to be fed back.		

Instruction name	The main code reads the secondary code		
Instruction code	0xF4	Instruction content	Instruction code + main code + CRC + square wave × 120
Content description	The main code field length is 8 bytes.		
Instruction function	The main code is correct, after the CRC check is passed: 13 bytes of secondary code are fed back in the square wave; after the secondary code feedback is completed, 1 byte CRC and 1 byte 0x80 are continued to be fed back.		

Instruction name	The main code reads the spare area		
Instruction code	0xF1	Instruction content	Instruction code + main code + CRC + square wave × 120
Content description	The main code field length is 8 bytes.		
Instruction function	The main code is correct, after the CRC check is passed: 13 bytes of spare area are fed back in the square wave; after the spare area feedback is completed, 1 byte CRC and 1 byte 0x80 are continued to be fed back.		

Instruction name	Master code verifies detonation password		
Instruction code	0xF7	Instruction content	Command code + master code + detonation password + CRC + square wave × 8
Content description	The length of the master code field is 8 bytes; the length of the detonation password field is 8 bytes.		
Instruction function	When the master code is correct and the CRC check passes: if the detonation password is correct, set the detonation password verification pass flag to 1. When the master code is correct and the CRC check passes: if the detonation password is correct, feedback 1 byte 0xAA in the square wave; if the detonation password is incorrect, feedback 1 byte 0xFF in the square wave.		

Instruction name	Master code checks for open resistance		
Instruction code	0xE6	Instruction content	Command code + master code + parameter + CRC + square wave × (T + 2) × 8
Content description	The length of the master code field is 8 bytes; the length of the parameter field is 1 byte, defined as follows:		
Instruction function	When the master code is correct and the CRC check passes: if the charging switch is off and the discharging switch is on, turn on the energy storage capacitor voltage comparator. The master code is correct, and after the CRC check passes: When the falling edge of the first square wave is received: set the resistance open circuit checked flag and the resistance open circuit check passed flag to 0; if the charging switch is off, the discharging switch is on, and the energy storage capacitor voltage is less than 3V, turn off the discharging switch, turn on the NMOS firing switch, and then turn on the resistance measurement circuit. Between the falling edge of the first square wave and the rising edge of the (T×8+9)th square wave: if the resistance voltage reaches the voltage specified by the "Resistance Reference Voltage Selection" field in the configuration area, or the energy storage capacitor voltage reaches 3V, turn off the NMOS firing switch, turn off the resistance measurement circuit, turn on the discharging switch, and turn off the energy storage capacitor voltage comparator. When receiving the rising edge of the (T×8+9)th square wave: set the resistance open circuit checked flag to 1; if the resistance measurement circuit is still working, set the resistance open circuit check passed flag to 1; turn off the NMOS ignition switch, turn off the resistance measurement circuit, turn on the discharge switch, and turn off the energy storage capacitor voltage comparator. In the (T×8+9)th to (T×8+16)th square waves: if the resistance open circuit check passed flag is 0, then feedback 1 byte 0xFF; if the resistance open circuit check passed flag is 1, then feedback 1 byte 0xAA.		
Notes	● When the energy storage capacitor is normal, if T is too small, the resistance open circuit may not be detected		

Bit	Definition
[7:4]	Undefined
[3:0]	Timing of ending the check T 0~15 End the check and start feedback at the rising edge of the (T×8+9)th square wave

<table>
<tr><td>Instruction name</td><td colspan="3">Master code to check the capacitor open circuit</td></tr>
<tr><td>Instruction code</td><td>0xE5</td><td>Instruction content</td><td>Instruction code + master code + parameter + CRC + square wave × (T × 2 + 8)</td></tr>
<tr><td>Content description</td><td colspan="3">The length of the master code field is 8 bytes; the length of the parameter field is 1 byte, defined as follows:
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>[7:4]</td><td>Undefined</td></tr>
<tr><td>[3:1]</td><td>Timing of ending the check T
0~7 end the check and start feedback at the (T×2+1)th square wave rising edge</td></tr>
<tr><td>[0]</td><td>Charging position, 0 3V position, 1 5V position</td></tr>
</table></td></tr>
<tr><td>Instruction function</td><td colspan="3">When the master code is correct and the CRC check passes: set the capacitor open circuit checked flag and the capacitor open circuit check failed flag to 0; if the charging switch is off and the discharge switch is on, turn off the discharge switch, turn on the charging switch, drill the energy storage capacitor voltage comparator and select the reference voltage according to the charging gear specified in the parameter.
The master code is correct, and after the CRC check passes:
When the rising edge of the (T × 2 + 1)th square wave is received: if the capacitor open circuit check is in progress, turn off the charging switch, turn on the discharge switch, turn off the energy storage capacitor voltage comparator, and set the capacitor open circuit checked flag to 1; if the capacitor open circuit check is in progress and the energy storage capacitor is not fully charged, set the capacitor open circuit check passed flag to 1. In the (T×2+1)th to 24th square waves: if the capacitor open circuit check passed flag is 1, then 1 and 0 are alternately fed back in the square wave; if the capacitor open circuit check passed flag is 0, then 1 is fed back in each square wave.</td></tr>
</table>

<table>
<tr><td>Instruction name</td><td colspan="3">Master code charge/discharge</td></tr>
<tr><td>Instruction code</td><td>0xDD</td><td>Instruction content</td><td>Instruction code + master code + parameter + CRC</td></tr>
<tr><td>Content description</td><td colspan="3">The length of the master code field is 8 bytes; the length of the parameter field is 1 byte, defined as follows:
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>[7:4]</td><td>Undefined</td></tr>
<tr><td>[3:0]</td><td>Charging position, 1~9 3V, 5V, 10V, 12V, 14V, 16V, 18V, 20V, 22V,
Others discharge</td></tr>
</table></td></tr>
<tr><td>Instruction function</td><td colspan="3">When the master code is correct and the CRC check passes: set the current full charge flag to 0; if the charging gear specified in the parameter is not discharge, turn off the discharge switch, turn on the charge switch, turn on the energy storage capacitor voltage comparator and select the reference voltage according to the charging gear specified in the parameter; if the charging gear specified in the parameter is discharge, turn off the charge switch, turn on the discharge switch, turn off the energy storage capacitor voltage comparator, and set the once fully charged flag to 0.
When fully charged: set the once fully charged flag and the current fully charged flag to 1, and perform a direct feedback.</td></tr>
</table>

Appendix 2.2 A2 Class Instructions (Instructions Addressed by Number Value)

Instruction name	Number Value Writes Field Value		
Instruction code	0xA1	Instruction content	Instruction Code + Number Value + Delay Value + CRC + Square Wave × 8
Content description	Number Value Field Length is 2 bytes; Delay Value Field Length is 2 bytes.		
Instruction function	When the number value is correct and the CRC check passes: set the scan read flag to 1; store the delay value field in the instruction into the delay value register. When the number value is correct and the CRC check passes: the square wave feedback is 0xAA in the square wave.		

Instruction name	Number value reads detonator information		
Instruction code	0xA2	Instruction content	Command code + number value + parameter + CRC + square wave × (N + 2) × 8
Content description	The length of the number value field is 2 bytes; the length of the parameter field is 1 byte, defined as follows: Bit / Definition [7] 1 Feedback number value register (2 bytes), 0 No feedback [6] 1 Feedback delay value register (2 Byte), 0 No feedback [5] 1 Short spare area feedback (2 bytes), 0 No feedback [4] 1 Version number feedback (2 bytes), 0 No feedback [3] 1 Feedback calibration value register (2 bytes), 0 No feedback [2] 1 Feedback status register (2 bytes), 0 No feedback [1:0] Undefined N is the number of bytes of information specified by the parameter field.		
Instruction function	The number value is correct, after the CRC check is passed: according to the order of each bit in the parameter from high to low, the information specified by the parameter field is fed back in the square wave; after the information feedback is completed, the scan read flag is set to 1, and 1 byte CRC and 1 byte 0x80 are continued to be fed back.		

Instruction name	Number value reads secondary code		
Instruction code	0xB6	Instruction content	Command code + number value + CRC + square wave × 120
Content description	The length of the number value field is 2 bytes.		
Instruction function	The number value is correct, after the CRC check is passed: 13 bytes of secondary code are fed back in the square wave; after the secondary code feedback is completed, 1 byte CRC and 1 byte 0x80 are continued to be fed back.		

Instruction name	Number value reads spare area		
Instruction code	0xB9	Instruction content	Command code + number value + CRC + square wave × 120

Content description	The length of the number value field is 2 bytes.
Instruction function	Number value is correct, after CRC check is passed: feedback 13 bytes of spare area in square wave; after spare area feedback is completed, continue to feedback 1 byte CRC and 1 byte 0x80.

Instruction name	Number value verifies detonation password		
Instruction code	0xAB	Instruction content	Instruction code + number value + detonation password + CRC + square wave × 8
Content description	Number value field length is 2 bytes; detonation password field length is 8 bytes.		
Instruction function	Number value is correct, when CRC check is passed: if the detonation password is correct, set the detonation password verification pass flag to 1. Number value is correct, after CRC check is passed: if the detonation password is correct, feedback 1 byte 0xAA in square wave; if the detonation password is incorrect, feedback 1 byte 0xFF in square wave.		

Instruction name	Number value check resistor open circuit		
Instruction code	0xBA	Instruction content	Command code + number value + parameter + CRC + square wave × (T + 2) × 8
Content description	The length of the number value field is 2 bytes; the length of the parameter field is 1 byte, defined as follows: Bit: [7:4] Undefined Bit: [3:0] Timing of ending the check T 0~15 End the check and start feedback at the rising edge of the (T×8+9)th square wave		
Instruction function	Number value is correct, when CRC check passes: If the charging switch is off and the discharging switch is on, then turn on the energy storage capacitor voltage comparator. Number value is correct, after CRC check passes: When the falling edge of the first square wave is received: set the resistance open circuit checked flag and the resistance open circuit check passed flag to 0; if the charging switch is off, the discharging switch is on, and the energy storage capacitor voltage is less than 3V, turn off the discharging switch, turn on the NMOS firing switch, and then turn on the resistance measurement circuit. Between the falling edge of the first square wave and the rising edge of the (T×8+9)th square wave: if the resistance voltage reaches the voltage specified by the "Resistance Reference Voltage Selection" field in the configuration area, or the energy storage capacitor voltage reaches 3V, turn off the NMOS firing switch, turn off the resistance measurement circuit, turn on the discharging switch, and turn off the energy storage capacitor voltage comparator. When receiving the rising edge of the (T×8+9)th square wave: set the resistance open circuit checked flag to 1; if the resistance measurement circuit is still working, set the resistance open circuit check passed flag to 1; turn off the NMOS ignition switch, turn off the resistance measurement circuit, turn on the discharge switch, and turn off the energy storage capacitor voltage comparator. In the (T×8+9)th to (T×8+16)th square waves: if the resistance open circuit check passed flag is 0, then feedback 1 byte 0xFF; if the resistance open circuit check passed flag is 1, then feedback 1 byte 0xAA.		
Notes	● When the energy storage capacitor is normal, if T is too small, the resistance open circuit may not be detected		

<table>
<tr><td>Instruction name</td><td colspan="3">Number value check capacitor open circuit</td></tr>
<tr><td>Instruction code</td><td>0xBF</td><td>Instruction content</td><td>Command code + number value + parameter + CRC + square wave × (T × 2 + 8)</td></tr>
<tr><td>Content description</td><td colspan="3">The length of the number value field is 2 bytes; the length of the parameter field is 1 byte, defined as follows:
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>[7:4]</td><td>Undefined</td></tr>
<tr><td>[3:1]</td><td>Timing of ending the check T
0~7 end the check and start feedback at the (T×2+1)th square wave rising edge</td></tr>
<tr><td>[0]</td><td>Charging position, 0 3V position, 1 5V position</td></tr>
</table></td></tr>
<tr><td>Instruction function</td><td colspan="3">Number value is correct, when CRC check passes: Set the capacitor open circuit checked flag and the capacitor open circuit check failed flag to 0; if the charging switch is off and the discharging switch is on, turn off the discharging switch, turn on the charging switch, drill the energy storage capacitor voltage comparator and select the reference voltage according to the charging gear specified in the parameter.
Number value is correct, after CRC check passes:
When the rising edge of the (T × 2 + 1)th square wave is received: if the capacitor open circuit check is in progress, turn off the charging switch, turn on the discharge switch, turn off the energy storage capacitor voltage comparator, and set the capacitor open circuit checked flag to 1; if the capacitor open circuit check is in progress and the energy storage capacitor is not fully charged, set the capacitor open circuit check passed flag to 1. In the (T×2+1)th to 24th square waves: if the capacitor open circuit check passed flag is 1, then 1 and 0 are alternately fed back in the square wave; if the capacitor open circuit check passed flag is 0, then 1 is fed back in each square wave.</td></tr>
</table>

<table>
<tr><td>Instruction name</td><td colspan="3">Number value charge/discharge</td></tr>
<tr><td>Instruction code</td><td>0x87</td><td>Instruction content</td><td>Command code + number value + parameter + CRC</td></tr>
<tr><td>Content description</td><td colspan="3">The length of the number value field is 2 bytes; the length of the parameter field is 1 byte, defined as follows:
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>[7:4]</td><td>Undefined</td></tr>
<tr><td>[3:0]</td><td>Charging position, 1~9 3V, 5V, 10V, 12V, 14V, 16V, 18V, 20V, 22V,
Others discharge</td></tr>
</table></td></tr>
<tr><td>Instruction function</td><td colspan="3">Number value is correct, when CRC check passes: set the current fully charged flag to 0; if the charging gear specified in the parameter is not discharge, turn off the discharge switch, turn on the charge switch, turn on the energy storage capacitor voltage comparator and select the reference voltage according to the charging gear specified in the parameter; if the charging gear specified in the parameter is discharge, turn off the charge switch, turn on the discharge switch, turn off the energy storage capacitor voltage comparator, and set the fully charged flag to 0.
When fully charged: set the once fully charged flag and the current fully charged flag to 1, and perform a direct feedback.</td></tr>
</table>

Appendix 2.3 Class B instructions (broadcast instructions used on site)

Instruction name	Clear read		
Instruction code	0x1F2A	Instruction content	Command code + CRC
Instruction function	When CRC check passes: set the scan read flag to 0 and clear the general counter.		

Instruction name	Scan		
Instruction code	0x7A	Instruction content	Instruction code + parameter + CRC + square wave × (N + 10) × 8
Content description	The parameter field length is 1 byte, defined as follows: Bit: Definition [7]: 1 Feedback number value register (2 bytes), 0 No feedback [6]: 1 Feedback delay value register (2 Byte), 0 No feedback [5]: 1 Short spare area feedback (2 bytes), 0 No feedback [4]: 1 Version number feedback (2 bytes), 0 No feedback [3]: 1 Feedback calibration value register (2 bytes), 0 No feedback [2]: 1 Feedback status register (2 bytes), 0 No feedback [1]: Undefined [0]: 1 Enable automatic numbering function, 0 Disable automatic numbering function N is the number of bytes of information specified by the parameter field.		
Instruction function	After the CRC check passes: If the scanned read flag is 0, the main code is fed back in the square wave; then the information specified by the parameter field is fed back in the order from high to low in the parameter; then 1 byte CRC and 1 byte 0x40 are fed back. During the entire feedback process, if a bus conflict is detected, the feedback is stopped (see **9.2 Scan anti-collision mechanism**)。 If the "Enable automatic numbering function" in the parameter is 1, the automatically assigned number value will be written into the number value register after the main code is fed back. When the highest bit of the feedback completion 0x40 byte: Set the scan read flag to 1.		
Notes	● If you want to use the automatic numbering function, you must first send the "clear read" command, and then continuously send the "scan" command until the command no longer receives feedback.		

Instruction name	Software reset		
Instruction code	0x1966	Instruction content	Command code + CRC
Instruction function	When the CRC check passes: Execute software reset		

Instruction name	Delayed calibration		
Instruction code	0x2E2D	Instruction content	Command code + CRC + square wave × 129
Instruction function	After the CRC check passes: When the rising edge of the first square wave is received: If the delayed calibration completion flag is 0, start calibration. When the rising edge of the 129th square wave is received: End calibration, set the delayed calibration completion flag to 1.		
Notes	● The average period of the square wave should be 1±0.001ms, and the duty cycle should be 1:1.		

Instruction name	Verify the detonation password		
Instruction code	0x28	Instruction content	Command code + detonation password + CRC + square wave × 8
Content description	The detonation password field length is 8 bytes.		
Instruction function	When the CRC check passes: If the detonation password is correct, set the detonation password verification pass flag to 1. After the CRC check passes: If the detonation password is correct, feedback 1 byte 0xAA in the square wave; if the detonation password is incorrect, no feedback is given.		

Instruction name	Charge/discharge		
Instruction code	0x41	Instruction content	Command code + number value + parameter + CRC
Content description	The length of the number value field is 2 bytes, and the length of the parameter field is 3 bytes, which are defined as follows:		

Bit	Definition
[23:16]	Delay value matching interval lower limit L 0~255 Charge only when the delay value in the chip is greater than or equal to (L×256)
[15:8]	Delay value matching interval upper limit H 0~255 Charge only when the delay value in the chip is less than or equal to (H×256)
[7:4]	Number of digits matching the number value N 0~15 Charging is performed only when the high (16-N) bit of the number value in the chip is consistent with the high (16-N) bit of the number value in the instruction
[3:0]	Charging position, 1~9 3V, 5V, 10V, 12V, 14V, 16V, 18V, 20V, 22V, Others discharge

Instruction function	When the number value matches correctly, the extension value matches correctly, and the CRC check passes: set the current full charge flag to 0; if the charging gear specified in the parameter is not discharge, turn off the discharge switch, turn on the charge switch, turn on the energy storage capacitor voltage comparator and select the reference voltage according to the charging gear specified in the parameter; if the charging gear specified in the parameter is discharge, turn off the charge switch, turn on the discharge switch, turn off the energy storage capacitor voltage comparator, and set the once fully charged flag to 0. When fully charged: set the once fully charged flag and the current fully charged flag to 1.

Instruction name	Get all verification status		
Instruction code	0x27	Instruction content	Instruction code + parameter + CRC + square wave × 8

Content description

The parameter field length is 1 byte, defined as follows:

Bit	Definition
[7]	Calibration value write flag, 1 check, 0 do not check
[6]	Configuration area write flag, 1 check, 0 do not check
[5]	Detonation password verification passed flag, 1 check, 0 do not check
[4]	Fully charged flag, 1 check, 0 do not check
[3]	Deferred calibration completed flag, 1 check, 0 do not check
[2]	Currently fully charged flag, 1 check, 0 do not check
[1]	Resistance open circuit check passed flag, 1 check, 0 do not check
[0]	Capacitor open circuit check passed flag, 1 check, 0 do not check

Instruction function	After CRC check: If the flag bits specified by the parameter field to be checked are not all 1, 0xFF is fed back in the square wave.

Instruction name	Get the verification status of each shot		
Instruction code	0x24	Instruction content	Instruction code + number value offset + parameter + CRC + square wave × N

Content description

The number value offset field length is 2 bytes. The parameter field length is 1 byte, defined as follows:

Bit	Definition
[7]	Calibration value write flag, 1 check, 0 do not check
[6]	Configuration area write flag, 1 check, 0 do not check
[5]	Detonation password verification passed flag, 1 check, 0 do not check
[4]	Fully charged flag, 1 check, 0 do not check
[3]	Deferred calibration completed flag, 1 check, 0 do not check
[2]	Currently fully charged flag, 1 check, 0 do not check
[1]	Resistance open circuit check passed flag, 1 check, 0 do not check
[0]	Capacitor open circuit check passed flag, 1 check, 0 do not check

N is (maximum number value to be checked - number value offset).

Instruction function	After CRC check: If the flag bits specified by the parameter field to be checked are all 1, 1 is fed back in the (number value register - number value offset)th square wave.
Notes	● If the parameter field is 0x00, 1 is fed back in the (number value register - number value offset)th square wave regardless of the status byte.

Instruction name	Detonation		
Instruction code	0x3CC8	Instruction content	Instruction code + parameter + CRC + square wave × N
Content description	The parameter field length is 1 byte, defined as follows: Bit: [7:0] — Definition: Countdown before extension D 0~255 Start extension after (D×256)ms after CRC check passes N is the largest number value in the networking chip.		
Instruction function	When the CRC check passes: If the detonation conditions are met (i.e., the detonation password verification passed flag, the fully charged flag, and the extended calibration completed flag are all 1), and the countdown before extension specified in the parameter is 0, then the extension begins; if the detonation conditions are met, and the countdown before extension specified in the parameter is not 0, then the countdown before detonation begins. After the CRC check passes: If the detonation conditions are met, 1 is fed back in the (number value register) square wave. At the end of the square wave: If the detonation conditions are not met, a software reset is executed.		

Instruction name	Set the test pin		
Instruction code	0x1A	Instruction content	Instruction code + parameter + CRC
Content description	The parameter field length is 1 byte.		
Instruction function	When the CRC check passes: Set the test pin according to the parameter.		

Instruction name	Set configuration area		
Instruction code	0x42	Instruction content	Instruction code + configuration area + CRC
Content description	The length of the configuration area field is 3 bytes.		
Instruction function	When the CRC check passes: store the configuration area field in the instruction into the configuration area register.		

Instruction name	Check for open resistors		
Instruction code	0x75	Instruction content	Command code + number value + parameter + CRC + square wave × (T + 2) × 8
Content description	The length of the number value field is 2 bytes. The length of the parameter field is 1 byte, defined as follows:		

Bit	Definition
[7:4]	Number of digits matching the number value N 0~15 The high (16-N) bit of the number value in the chip is consistent with the high (16-N) bit of the number value in the instruction before the check is performed
[3:0]	Timing of ending the check T 0~15 End the check and start feedback at the rising edge of the (T×8+9)th square wave

Instruction function	The number value matches correctly, and the CRC check passes: If the charging switch is off and the discharging switch is on, turn on the energy storage capacitor voltage comparator. The number value matches correctly, and the CRC check passes: When the falling edge of the first square wave is received: set the resistance open circuit checked flag and the resistance open circuit check passed flag to 0; if the charging switch is off, the discharging switch is on, and the energy storage capacitor voltage is less than 3V, turn off the discharging switch, turn on the NMOS firing switch, and then turn on the resistance measurement circuit. Between the falling edge of the first square wave and the rising edge of the (T×8+9)th square wave: if the resistance voltage reaches the voltage specified by the "Resistance Reference Voltage Selection" field in the configuration area, or the energy storage capacitor voltage reaches 3V, turn off the NMOS firing switch, turn off the resistance measurement circuit, turn on the discharging switch, and turn off the energy storage capacitor voltage comparator. When receiving the rising edge of the (T×8+9)th square wave: set the resistance open circuit checked flag to 1; if the resistance measurement circuit is still working, set the resistance open circuit check passed flag to 1; turn off the NMOS ignition switch, turn off the resistance measurement circuit, turn on the discharge switch, and turn off the energy storage capacitor voltage comparator. In the (T×8+9)th to (T×8+16)th square waves: if the resistance open circuit check passed flag is 0, then feedback 1 byte 0xFF; if the resistance open circuit check passed flag is 1, then feedback 1 byte 0xAA.
Notes	● When the energy storage capacitor is normal, if T is too small, the resistance open circuit may not be detected

<table>
<tr><td>Instruction name</td><td colspan="3">Check the capacitor open circuit</td></tr>
<tr><td>Instruction code</td><td>0x79</td><td>Instruction content</td><td>Command code + number value + parameter + CRC + square wave × (T × 2 + 8)</td></tr>
<tr><td>Content description</td><td colspan="3">The length of the number value field is 2 bytes. The length of the parameter field is 1 byte, defined as follows:
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>[7:4]</td><td>Number of digits matching the number value N
0~15 The high (16-N) bit of the number value in the chip is consistent with the high (16-N) bit of the number value in the instruction before the check is performed</td></tr>
<tr><td>[3:1]</td><td>Timing of ending the check T
0~7 end the check and start feedback at the (T×2+1)th square wave rising edge</td></tr>
<tr><td>[0]</td><td>Charging position, 0 3V position, 1 5V position</td></tr>
</table></td></tr>
<tr><td>Instruction function</td><td colspan="3">The number value matches correctly, and the CRC check passes: Set the capacitor open circuit checked flag and the capacitor open circuit check failed flag to 0; if the charging switch is off and the discharge switch is on, turn off the discharge switch, turn on the charging switch, drill the energy storage capacitor voltage comparator and select the reference voltage according to the charging gear specified in the parameter. The number value matches correctly, and the CRC check passes:
When the rising edge of the (T × 2 + 1)th square wave is received: if the capacitor open circuit check is in progress, turn off the charging switch, turn on the discharge switch, turn off the energy storage capacitor voltage comparator, and set the capacitor open circuit checked flag to 1; if the capacitor open circuit check is in progress and the energy storage capacitor is not fully charged, set the capacitor open circuit check passed flag to 1. In the (T×2+1)th to 24th square waves: if the capacitor open circuit check passed flag is 1, then 1 and 0 are alternately fed back in the square wave; if the capacitor open circuit check passed flag is 0, then 1 is fed back in each square wave.</td></tr>
</table>

<table>
<tr><td>Instruction name</td><td colspan="3">Check the version number</td></tr>
<tr><td>Instruction code</td><td>0x7F</td><td>Instruction content</td><td>Instruction code + version number + CRC + square wave × 8</td></tr>
<tr><td>Content description</td><td colspan="3">The length of the version number field is 2 bytes.</td></tr>
<tr><td>Instruction function</td><td colspan="3">After the CRC check is passed: if the version number in the instruction is the same as the version number in the chip, 0x0F is fed back in the square wave; if the version number in the instruction is different from the version number in the chip, 0xF0 is fed back in the square wave.</td></tr>
</table>

Appendix 2.4 Class C instructions (test instructions)

Instruction name	Write master code		
Instruction code	0x1E	Instruction content	Instruction code + master code + CRC
Content description	The main code field length is 8 bytes.		
Instruction function	When the CRC check is passed: write the master code field in the instruction to NVM. When NVM writing is completed: perform a direct feedback.		

Instruction name	Write detonation password		
Instruction code	0x1D	Instruction content	Instruction code + detonation password + CRC
Content description	The detonation password field length is 8 bytes.		
Instruction function	When the CRC check is passed: write the detonation password field in the instruction to NVM. When NVM writing is completed: perform a direct feedback.		

Instruction name	Write secondary code		
Instruction code	0x1B	Instruction content	Instruction code + secondary code + CRC
Content description	The secondary code field length is 13 bytes.		
Instruction function	When the CRC check passes: write the secondary code field in the instruction to NVM. When NVM writing is completed: perform a direct feedback.		

Instruction name	Write live value		
Instruction code	0x18	Instruction content	Instruction code + number value + extension value + short spare area + CRC
Content description	The number value field length is 2 bytes. The extension value field length is 2 bytes. The short spare area field length is 2 bytes.		
Instruction function	When the CRC check passes: store the number value and extension value fields in the instruction into the number value and extension value registers, and write the number value, extension value, and short spare area fields in the instruction to NVM. When NVM writing is completed: perform a direct feedback.		

Instruction name	Write spare area		
Instruction code	0x12	Instruction content	Instruction code + spare area + CRC
Content	The spare area field length is 13 bytes.		

description	
Instruction function	When the CRC check passes: write the spare area field in the instruction to NVM. When NVM writing is completed: perform a direct feedback.

Instruction name	Write version number and configuration area		
Instruction code	0x14	Instruction content	Instruction code + version number + configuration area + configuration area CRC + CRC
Content description	The length of the version number field is 2 bytes. The length of the configuration area field is 3 bytes. The length of the configuration area CRC field is 1 byte.		
Instruction function	When the CRC check passes: store the configuration area field in the instruction into the configuration area register, and write the version number, configuration area, and configuration area CRC fields in the instruction into NVM. When NVM writing is completed: perform a direct feedback.		

Instruction name	Read secondary code		
Instruction code	0x2C	Instruction content	Instruction code + CRC + square wave × 120
Instruction function	After the CRC check passes: feedback 13 bytes of secondary code in the square wave; after the secondary code feedback is completed, continue to feedback 1 byte CRC and 1 byte 0x80.		

Instruction name	Read the field value		
Instruction code	0x22	Instruction content	Instruction code + CRC + square wave × 64
Instruction function	After the CRC check is passed: feedback 2 bytes of number value, 2 bytes of extension value, 2 bytes of short spare area in the square wave; after the short spare area feedback is completed, continue to feedback 1 byte CRC and 1 byte 0x80.		

Instruction name	Read the spare area		
Instruction code	0x37	Instruction content	Instruction code + CRC + square wave × 120
Instruction function	After the CRC check is passed: feedback 13 bytes of spare area in the square wave; after the spare area feedback is completed, continue to feedback 1 byte CRC and 1 byte 0x80.		

Instruction name	Read the version number and configuration area		
Instruction code	0x34	Instruction content	Instruction code + CRC + square wave × 56
Instruction function	After the CRC check is passed: feedback 2 bytes of version number and 3 bytes of configuration area (from the configuration area register) in the square wave; after the configuration area feedback is completed, continue to feedback 1 byte CRC and 1 byte 0x80.		

Instruction name	Read version number and configuration area NVM		
Instruction code	0x35	Instruction content	Instruction code + CRC + square wave × 64
Instruction function	After CRC check: feedback 2 bytes of version number, 3 bytes of configuration area (from NVM), 1 byte of configuration area CRC in the square wave; after the configuration area feedback is completed, continue to feedback 1 byte CRC and 1 byte 0x80.		

Instruction name	Lock		
Instruction code	0x16	Instruction content	Command code + CRC
Instruction function	When CRC check passes: set the lock flag to 1 and write to NVM. When NVM writing is completed: perform a direct feedback.		